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PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM MANUAL

VOLUME I OF II

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER

BY

AC ELECTRONICS
DIVISION OF GENERAL MOTORS
MILWAUKEE,WISCONSIN 53201

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			4-512, 4-513 thru 4-518, 4-519/		
			4-520, 4-521, 4-522, 4-523/4-524,		
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			4-540, 4-541/4-542, 4-543/4-544,		
			4-545/4-546, 4-547/4-548, 4-549/		
			4-550, 4-551/4-552, 4-553/4-554,		
			4-555/4-556, 4-557 thru 4-560,		
			4-561/4-562, 4-563, 4-564, 4-565/		
			4-566, 4-567/4-568, 4-569/4-570,		
			4-571 thru 4-582, 4-583/4-584,		
			4-585/4-586, 4-587/4-588, 4-589/		
			4-590, 4-591/4-592, 4-593 thru		
			4-598, 4-599/4-600, 4-601/4-602,		
			4-603/4-604, 4-605/4-606, 4-607/		
			4-608, 4-609/4-610, 4-611/4-612,		
			4-613/4-614, 4-615, 4-616, 4-617/		
			4-618, 4-619, 4-620, 4-621/4-622,		
			4-623/4-624, 4-625/4-626, 4-627,		
			4-628, 4-629/4-630, 4-631/4-632,		
			4-633/4-634, 4-635 thru 4-650,		
			4-651/4-652, 4-653 thru 4-656,		
			4-657/4-658, 4-659/4-660, 4-661,		
			4-662, 4-663/4-664, 4-665, 4-666,		
			4-667/4-668, 4-669/4-670, 4-671/		
			4-672, 4-673/4-674, C-1 thru		
			C-7/C-8		

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				CCB	NASA
G	3-10-67	33199	Title (Vol. I)/Blank, I-ivE/	EA	
			1-ivF, I-vii thru I-viiiB, 1-ix		
			thru I-xA/I-xB, I-xv, I-xvi,		
			I-xxxi thru I-xxxvi, 7-37, 7-38,		
			Title (Supplement)/Blank, S-iii/		
			S-iv, S-v/S-vi, S-1/S-2 thru		
			S-31/S-32, S-33 thru S-57/		
			S-58, S-59 thru S-77/S-78,		
			S-79 thru S-85/S-86, S-87 thru		
			S-103/S-104, S-105 thru		
			S-127/S-128, S-129 thru S-148		
H	4-20-67	33649	Title (Vol. I)/Blank, I-ivE/	EA	
			I-ivF, I-vii thru I-viiiB, I-ix		
			thru I-xA/I-xB, I-xii, I-xviii,		
			1-xxv thru I-xxviA/I-xxviB,		
			I-xxxC/I-xxxD, 3-1 thru 3-2U/		
			3-2V, 3-3, 3-5, 3-10, 3-22,		
			7-17/7-18, 7-19/7-20, 7-21/		
			7-22, 7-23/7-24, 7-25/7-26,		
			7-27/7-28, 7-29/7-30, 7-33/		
			7-34, 7-35/7-36, 7-39/7-40,		
			8-1 thru 8-3/8-4, 8-8 thru		
			8-11/8-12, 8-14		
J	5-12-67	33781	Title/I-ii, I-ivE, I-ivF, I-vii thru	EA	
			1-viiiB, 1-ix thru 1-xA/I-xB,		

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				CCB	NASA
			I-xviii, I-xxi, I-xxxC thru		
			I-xxxF, 3-2L, 3-2M, 3-3,		
			3-4A/3-4B, 4-222A/4-222B,		
			4-222C/4-222D, 4-222E/4-222F,		
			4-223/4-224, 4-229, 4-232A/		
			4-232B, 4-232C/4-232D, 4-593,		
			4-619, 4-659/4-660, 6-6 thru		
			6-10B		
K	6-1-67	33900	Title/I-ii, I-ivF, I-vii thru	EA	
			I-viiiB, I-ix thru I-xA/I-xB,		
			I-xxv, I-xxxF, I-xxxG/I-xxxH,		
			3-2A thru 3-2C, 3-2F thru		
			3-2I, 3-2N thru 3-2AA/3-2AB,		
			4-593, 4-619		
L	6-30-67	34071	Title/I-ii, I-ivF, I-vii thru	EA	
			I-viiiB, I-ix thru I-xA/I-xB,		
			I-xiii, I-xiv, I-xviii, I-xxiv, I-xxv,		
			I-xxvii, 3-2A, 3-2D, 3-2E, 3-2J,		
			3-2K, 3-12, 3-22, 3-22A/3-22B,		
			3-24 thru 3-24D, II-iii, II-viA,		
			II-ix/II-x, 4-675 thru 4-683/		
			4-684, 4-685/4-686, 4-687, 4-688,		
			7-35/7-36, 8-7, 8-8, A-1 thru		
			A-9/A-10		

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				CCB	NASA
M	8-4-67	34291	Title/I-ii, I-ivG/I-ivH, I-vii	EA	
			thru I-viiiB, I-ix thru I-xA/		
			I-xB, I-xxxG, I-xxxH, 3-2B		
			thru 3-2E, 3-2H thru 3-2M,		
			3-4, 3-21, 6-1 thru 6-2A/6-2B		
N	8-10-67	34303	Title/I-ii, I-ivG/I-ivH, I-vii	EA	
			thru I-viiiB, I-ix thru I-xA/		
			I-xB, I-xv, I-xxviii, II-iv,		
			II-ix/II-x, 7-1, 7-2 thru 7-2L		
P	8-17-67	34356	Title/I-ii, I-ivG/I-ivH, I-vii,	EA	
			I-viii, I-viiiA, I-viiiB, I-ix, I-x,		
			I-xA/I-xB, I-xv, II-iv, 8-15/8-16		
R	9-7-67	34511	Title/I-ii, I-ivG/I-ivH, I-vii thru	EA	
			I-viiiB, I-ix thru I-xA/I-xB,		
			I-xv, I-xxviii, I-xxxH, I-xxxii		
			thru I-xxxivB, 3-2A, 3-2F, 3-2G,		
			3-2P thru 3-2R, II-iv, II-ix/II-x,		
			7-2L, 7-31/7-32, 7-39/7-40,		
			8-2 thru 8-2C/8-2D, 8-5 thru		
			8-6E/8-6F, 8-8, 8-8A/8-8B,		
			8-9, 8-13, 8-14, A-1		
S	9-21-67	34663	Title/I-ii, I-ivG, I-ivH, I-vii thru	EA	
			I-viiiB, I-ix thru I-xA/I-xB,		
			I-xxviii, I-xxxA thru I-xxxH,		
			I-xxxivA, 3-2A, 3-2C, 3-2E,		

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				CCB	NASA
			3-2I thru 3-2O, 3-2V thru		
			3-2Y, 6-3, 6-4, 7-1, 7-4 thru		
			7-4B, 7-5 thru 7-9, 8-7		
T	10-12-67	34856	Title/I-ii, I-ivH, I-vii thru	EA	-
			I-viiiB, I-ix thru I-xA/I-xB,		
			I-xxv, 2-35, 2-37, 3-2S,		
			3-21, 4-15, 4-19, 4-23,		
			4-34C/4-34D, 4-37, 5-1,		
			5-5, 7-19/7-20		
U	10-27-67	34962	Title/ii, I-ivH, I-vii thru I-viiiB,	EA	
			I-ix thru I-xB, I-xxiv, I-xxxI/		
			I-xxxiJ, 3-2A, 3-2F thru 3-2I,		
			4-50 thru 4-52, 4-59 thru 4-62,		
			4-64 thru 4-66, 4-73, 4-110 thru		
			4-112, 4-120, 4-121, 4-129,		
			4-130, 4-135, 4-142, 4-153,		
			4-158 thru 4-160, 4-162, 4-172,		
			4-175 thru 4-178, 4-251 thru		
			4-255, 4-407, 4-469/4-470,		
			4-471/4-472, 4-492, 4-498,		
			4-547/4-548, 4-620, 4-620A/		
			4-620B, 4-625/4-626, 4-626A/		
			4-626B, 4-626C, 4-626D, 4-627,		
			4-628, 4-629/4-630, 4-630A/		
			4-630B, 4-630C/4-630D, 8-14		

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				CCB	NASA
V	11-16-67	35039	Title/I-ii, I-ivI/I-ivJ, I-vii thru	EA	
			I-viiiB, I-ix thru I-xB, I-xii,		
			I-xviii, 3-2B thru 3-2E, 3-2G,		
			3-2I thru 3-2K, 3-2M, 3-2O,		
			3-2Q, 3-2U, 3-2W thru 3-2AA/		
			3-2AB, 3-11, 3-12A, 3-12C thru		
			3-12F, 3-26, 3-26A/3-26B,		
			7-4B		
W	12-14-67	35241	Title/I-ii, I-ivI/I-ivJ, I-vii thru	EA	
			I-viiiB, I-ix thru I-xB, I-xviiiA/		
			I-xviiiB, I-xxv, I-xxvi, I-xxxI/		
			I-xxxJ, 3-2A thru 3-2AA/		
			3-2AB, 3-25, 4-15, 4-44D,		
			4-45 thru 4-47/4-48, 4-48A/		
			4-48B, 4-48C thru 4-48AA/		
			4-48AB, 4-49, 8-9		
Y	1-19-68	35465	Title/I-ii, I-ivI/I-ivJ, I-vii	EA	
			thru I-viiiB, I-ix thru I-xB,		
			I-xv, I-xxxI/I-xxxJ, I-xxxii,		
			I-xxxivA/I-xxxivB, 3-2A thru		
			3-2E, 3-2J, 3-2K, 3-2V thru		
			3-2Y, II-iv, 6-2, 6-2A/6-2B,		
			6-3 thru 6-5, 7-4, 7-33/7-34,		
			8-3/8-4, 8-14, I-1 thru I-19/		
			I-20		

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				CCB	NASA
Z	2-15-68	35589	Title/ii (Vol. I), I-ivI, I-ivJ,	EA	
			I-vii thru I-viiiB, I-ix thru I-xB,		
			I-xv, I-xxivA/I-xxivB, I-xxviii,		
			I-xxxI, 3-2A, 3-2H, 3-2I, 3-2L,		
			3-2M, II-iv, II-viB, II-ix/II-x,		
			7-1, 7-2K, 7-2L, 7-16, 7-16A/		
			7-16B, 7-19/7-20, 7-25/7-26,		
			7-31/7-32, 7-33/7-34, 7-37,		
			7-39/7-40, 7-41/7-42, 7-43/		
			7-44, 7-45/7-46, 8-1, 8-3/8-4,		
			8-8, 8-8A/8-8B, 8-14		
AA	3-7-68	35852	Title/I-ii, I-ivJ, I-vii thru	EA	
			I-viiiB, I-ix thru I-xB, I-xviii,		
			3-20, 3-22A/3-22B, 3-24, 3-27,		
			3-29, 4-492, 4-498, 4-650, 4-653,		
			4-663/4-664, 4-669/4-670,		
			4-671/4-672, 7-2K, 8-6D thru		
			8-6F		
AB	4-29-68	36125	Title/I-ii, I-ivJ, I-vii thru	EA	
			I-viiiB, I-ix thru I-xB, I-xiii,		
			I-xviii, I-xxv, 3-2D, 3-2E, 3-2G,		
			3-21 thru 3-22M/3-22N, 4-513,		
			6-2A/6-2B, 6-3, 7-11 thru 7-15,		
			8-1, 8-2, 8-2B, 8-2C/8-2D, I-13		

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				CCB	NASA
AC	7-25-68	36590	Title/I-ii, I-ivK/I-ivL, I-vii thru I-viiiB, I-ix thru I-xB, I-xii, I-xviii, I-xxxI/I-xxxJ, 3-2A thru 3-2C, 3-11 thru 3-12E, 4-437, 4-481/4-482, 4-539, 6-1, 6-2, 6-4, 7-13, 7-16, 7-16A/7-16B, 7-21/7-22, 8-14	EA	
AD	11-4-68	36977	Title/I-ii, I-ivK/I-ivL, I-vii thru I-viii, I-xB, I-xxxI thru I-xxxJ, 3-2A, 3-2L thru 3-2Q, 7-19/7-20, 7-21/7-22, 8-2, 8-6E, 8-7, 8-14 thru 8-15/8-16	EA	
AE	12-16-68	37124	Title/I-ii, I-ivK/I-ivL, I-vii, I-viii, I-xxxJ, 3-2A, 3-2V, 3-2W	EA	
AF	1-20-69	37232	Title/I-ii, I-ivK/I-ivL, I-vii, I-xB, 7-16, 7-16A/7-16B, 8-8, 8-8A/8-8B	EA	
AG	8-11-69	37755	Title/I-ii, I-ivK/I-ivL, I-vii, I-viii, I-xxxA, I-xxxG, I-xxxH, I-xxxJ, 3-2A thru 3-2P, 3-2R thru 3-2U, 3-2W, 3-2X, 3-2Z	EA	

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				CCB	NASA
AH	5-26-70	38111	Title/I-ii, I-ivK, I-ivL, I-vii,	EA	
			I-viii, I-xiii, I-xxv, I-xxxJ,		
			3-2A, 3-2L, 3-2L-1/3-2L-2,		
			3-2M, 3-22M, 3-22N		
AJ	8-5-71	38455	Title/I-ii, I-ivL, I-vii, I-viii,	EA	
			I-xxxJ, 3-2A, 3-2F, 3-2G,		
			3-2H, 3-2I		

PREPARED BY	**TITLE**	**DATE**
	Technical Writer	31 January 1966
AC Electronics		
EXAMINED BY	**TITLE**	**DATE**
	Publications Supervisor	31 Jan 66
AC Electronics		
APPROVED BY	**TITLE**	**DATE**
	Field Operations	31 Jan 66
AC Electronics		
APPROVED BY	**TITLE**	**DATE**
	[illegible]	[illegible]
MIT/IL		
APPROVED BY	**TITLE**	**DATE**
	CCB	16 Feb 66
MIT/IL		
APPROVED BY	**TITLE**	**DATE**
	[illegible]	[illegible]
NASA/MSC		

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TOTAL NUMBER OF PAGES IN THIS PUBLICATION
IS 1364 CONSISTING OF THE FOLLOWING:

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I-ivC thru I-ivD Added	F
I-ivE	J
I-ivF	L
I-ivG	S
I-ivH	U
I-ivI	Z
I-ivJ	AB
I-ivK	AH
I-ivL	AJ
I-v	Original
I-vi Blank	Original
I-vii	AJ
I-viii	AJ
I-viiiA thru I-viiiB	AC
I-ix thru I-xA	AC
I-xB	AF
I-xi	B
I-xii	AC
I-xiii	AH
I-xiv	L
I-xv	Z
I-xvi	G
I-xvii	B
I-xviii	AC
I-xviiiA	W
I-xviiiB Blank	A
I-xix thru I-xx	Original
I-xxi	J
I-xxii thru I-xxiii	F
I-xxiv	U
I-xxivA	Z
I-xxivB Blank	F
I-xxv	AH
I-xxvi	W
I-xxviA Added	H
I-xxviB Blank	H
I-xxvii	L
I-xxviii	Z
I-xxix	Original
I-xxx Blank	Original
I-xxxA	AG
I-xxxB thru I-xxxF	S
I-xxxG thru I-xxxH	AG
I-xxxI	Z
I-xxxJ	AJ
I-xxxi	G
I-xxxii	Y
I-xxxiii thru I-xxxiv	R
I-xxxivA	Y
I-xxxivB Added	R
I-xxxv thru I-xxxvi Added	G
1-1	B
1-2	Original
1-3 thru 1-8	B
1-9	Original
1-10 thru 1-12	B
1-12A thru 1-12B Added	B
1-13 thru 1-16	Original
1-17 Added	B
1-18 Blank	B
2-1 thru 2-5	B
2-6 thru 2-19	Original
2-20	A
2-21 thru 2-23	B
2-24 Blank	Original
2-24A Added	B
2-24B Blank	B
2-24C Added	B
2-24D Blank	B
2-25 thru 2-26	B
2-27	Original
2-28 Blank	Original
2-29 thru 2-31	Original
2-32 Blank	Original
2-33	A
2-34	Original
2-35	T
2-36	B
2-37	T
2-38	Original
2-39	B
2-40	Original
2-41 thru 2-42	B
2-42A Added	B

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Page No.	Rev.
2-42B Blank	B
2-43	B
2-44 Blank	Original
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2-46 thru 2-60	Original
3-1 thru 3-2	H
3-2A	AJ
3-2B thru 3-2E	AG
3-2F thru 3-2I	AJ
3-2J thru 3-2K	AG
3-2L	AH
3-2L-1 Added	AH
3-2L-2 Added	AH
3-2M	AH
3-2N thru 3-2P	AG
3-2Q	AD
3-2R thru 3-2U	AG
3-2V	AE
3-2W thru 3-2X	AG
3-2Y	Y
3-2Z	AG
3-2AA	W
3-2AB Blank	K
3-3	J
3-4	M
3-4A Added	J
3-4B Blank	J
3-5	H
3-6	C
3-6A Added	C
3-6B Blank	C
3-7 thru 3-8	Original
3-9	B
3-10	H
3-11 thru 3-12E	AC
3-12F	V
3-13	Original
3-14	B
3-15	C
3-16	Original
3-17	F
3-18 thru 3-19	B
3-20	AA
3-21 thru 3-22B	AB
3-22C thru 3-22L Added	AB
3-22M thru 3-22N	AH
3-23	Original
3-24	AA
3-24A thru 3-24D Added	L
3-25	W
3-26	V
3-26A Added	V
3-26B Blank	V
3-27	AA
3-28	F
3-29	AA
3-30	B
4-1 thru 4-14	Original
4-15	W
4-16 thru 4-18	Original
4-19	T
4-20 thru 4-21	B
4-22	Original
4-23	T
4-24 thru 4-25	Original
4-26	A
4-27 thru 4-28	Original
4-29 thru 4-30	A
4-31	Original
4-32 thru 4-34	A
4-34A Added	A
4-34B Blank	A
4-34C	T
4-34D Blank	A
4-34E Added	A
4-34F Blank	A
4-34G thru 4-34I Added	A
4-34J Blank	A
4-34K Added	A
4-34L Blank	A
4-34M thru 4-34O Added	A
4-34P Blank	A
4-34Q thru 4-34S Added	A
4-34T Blank	A
4-34U Added	A
4-34V Blank	A

LIST OF EFFECTIVE PAGES (cont)

Page No.	Rev.
4-34W Added	A
4-34X Blank	A
4-34Y thru 4-34AA Added	A
4-34AB Blank	A
4-34AC thru 4-34AE Added	A
4-34AF Blank	A
4-34AG thru 4-34AI Added	A
4-34AJ Blank	A
4-34AK thru 4-34AM Added	A
4-34AN Blank	A
4-34AO thru 4-34AS Added	A
4-34AT Blank	A
4-34AU thru 4-34AV Added	A
4-35 thru 4-36	A
4-37	T
4-38 thru 4-40	Original
4-41 thru 4-42	A
4-42A thru 4-42B Added	A
4-43	C
4-44	B
4-44A thru 4-44C Added	B
4-44D	W
4-45 thru 4-47	W
4-48 Blank	W
4-48A Added	W
4-48B Blank	W
4-48C thru 4-48AA Added	W
4-48AB Blank	W
4-49	W
4-50 thru 4-52	U
4-53 thru 4-58	Original
4-59 thru 4-62	U
4-63	Original
4-64 thru 4-66	U
4-67 thru 4-72	Original
4-73	U
4-74 thru 4-78	Original
4-79	F
4-80 Blank	Original
4-81	Original
4-82 Blank	Original
4-83	Original
4-84 Blank	Original
4-85	Original
4-86 Blank	Original
4-87	Original
4-88 Blank	Original
4-89	Original
4-90 Blank	Original
4-91	Original
4-92 Blank	Original
4-93	Original
4-94 Blank	Original
4-95	Original
4-96 Blank	Original
4-97	Original
4-98 Blank	Original
4-99	Original
4-100 Blank	Original
4-101	Original
4-102 Blank	Original
4-103	Original
4-104 Blank	Original
4-105	Original
4-106 Blank	Original
4-107 thru 4-109	Original
4-110 thru 4-112	U
4-113 thru 4-119	Original
4-120 thru 4-121	U
4-122 thru 4-128	Original
4-129 thru 4-130	U
4-131 thru 4-134	Original
4-135	U
4-136 thru 4-141	Original
4-142	U
4-143 thru 4-152	Original
4-153	U
4-154 thru 4-157	Original
4-158 thru 4-160	U
4-161	Original
4-162	U
4-163 thru 4-171	Original
4-172	U
4-173 thru 4-174	Original
4-175 thru 4-178	U
4-179 thru 4-203	Original
4-204 thru 4-205	F
4-206 Blank	Original
4-207	F

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Page No.	Rev.
4-208 Blank	Original
4-209	F
4-210 Blank	Original
4-211	F
4-212 Blank	Original
4-213	F
4-214 Blank	Original
4-215	F
4-216 Blank	Original
4-217	Original
4-218 Blank	Original
4-219	F
4-220 Blank	Original
4-221	F
4-222 Blank	Original
4-222A Added	J
4-222B Blank	J
4-222C Added	J
4-222D Blank	J
4-222E Added	J
4-222F Blank	J
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4-230	Original
4-231	F
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4-232B Blank	J
4-232C Added	J
4-232D Blank	J

Volume II

Page No.	Rev.
Title	B
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II-iii	L
II-iv	Z
II-v thru II-vi	F
II-viA	L
II-viB Added	Z
II-vii	Original
II-viii	F
II-ix	Z
II-x Blank	B
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4-238 thru 4-239	F
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4-241 thru 4-242	Original
4-243	F
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4-245	F
4-246 Blank	Original
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4-251 thru 4-255	U
4-256	Original
4-257	F
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4-269	F
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4-284 Blank	Original
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4-286 Blank	Original
4-287	F
4-288 Blank	Original

LIST OF EFFECTIVE PAGES
TOTAL NUMBER OF PAGES IN THIS PUBLICATION
IS 1266 CONSISTING OF THE FOLLOWING:

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Title	N
I-ii Blank	Original
I-iii thru I-iv	B
I-ivA thru I-ivB	F
I-ivC thru I-ivD Added	F
I-ivE	J
I-ivF	L
I-ivG	N
I-ivH Blank	M
I-v	Original
I-vi Blank	Original
I-vii thru I-viiiB	N
I-ix thru I-xA	N
I-xB Blank	F
I-xi	B
I-xii	H
I-xiii thru I-xiv	L
I-xv	N
I-xvi	G
I-xvii	B
I-xviii	L
I-xviiiA	B
I-xviiiB Blank	A
I-xix thru I-xx	Original
I-xxi	J
I-xxii thru I-xxiii	F
I-xxiv	L
I-xxivA Added	F
I-xxivB Blank	F
I-xxv	L
I-xxvi	H
I-xxviA Added	H
I-xxviB Blank	H
I-xxvii	L
I-xxviii	N
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I-xxxB	F
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I-xxxE Added	J
I-xxxF	K
I-xxxG thru I-xxxH	M
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I-xxxv thru I-xxxvi Added	G
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1-3 thru 1-8	B
1-9	Original
1-10 thru 1-12	B
1-12A thru 1-12B Added	B
1-13 thru 1-16	Original
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2-40	Original
2-41 thru 2-42	B
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2-43	B
2-44 Blank	Original
2-45	F
2-46 thru 2-60	Original
3-1 thru 3-2	H
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3-2B thru 3-2E	M
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3-4	M
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3-4B Blank	J
3-5	H
3-6	C
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3-7 thru 3-8	Original
3-9	B
3-10	H
3-11	E
3-12	L
3-12A	E
3-12B thru 3-12D	C
3-12E	E
3-12F Blank	B
3-13	Original
3-14	B
3-15	C
3-16	Original
3-17	F
3-18 thru 3-20	B
3-21	M
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3-23	Original
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3-24A thru 3-24D Added	L
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3-26	A
3-27	B
3-28 thru 3-29	F
3-30	B
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4-19 thru 4-21	B
4-22	Original
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4-29 thru 4-30	A
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Volume II

Title	B
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8-6E	AD
8-6F	AA
8-7	AD
8-8 thru 8-8A	AF
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8-9 thru 8-12 Deleted	Z
8-13	R
8-14 thru 8-15	AD
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C-7 Added	F
C-8 Blank	F
I-1 thru I-12 Added	Y
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SUPPLEMENT (limited distribution)

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LIST OF RELATED MANUALS

ND-1021038	Packing, Shipping and Handling Manual
ND-1021039	Auxiliary Ground Support Equipment Manual
ND-1021040	Bench Maintenance Ground Support Equipment Manual
ND-1021043	Block II Primary Guidance, Navigation, and Control System Manual

LIST OF ENGINEERING CHANGE PROPOSALS

Engineering change proposals (ECP's) which affect this manual and from which pertinent data has been incorporated are listed below. Unless otherwise specified, the ECP number listed is an AC Electronics ECP number.

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
172	GSE Statement of Work Change			Basic
179	GSE-PSA Filter Change			Basic
221	180 Degree Z IRIG Rotation			Basic
57	LEM Dimming Circuit			B
86	Additional GSE Items			B
204	Block II Temperature Control Change			B
306	IMU Harness Cable Clamp	102636	8102658	B
361	Exhibit D Statement of Work Change			B
388	Corrosion Protection	102645 102648 102650 102651 102652	8102670 8102674 8102676 8102677 8102678	B

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
197R2	Vacuum Testing of AOT			C
248	Pulse Torque Power Supply Redesign	102640	8102663	C
340	Navigation Base Redesign			C
360	Addition of AOT Cam Lock			C
321	AOT Eyepiece Heater Addition			C
421	Eyepiece Redesign to Provide Long Eye Relief Capability			C
389	ECP of Record for Improved Protective Covers for Cables (PN 2014137-011 and PN 2014199-011)			E
410	Relocation of AOT Focus Adjustment Cam Lock			E
422	CCRD Mounting Change			E
473	Pseudo Field Stop to Eliminate Light Scatter from the Radar Mount			E
226	Aluminum to Magnesium Conversion of Computer Trays			F
254	Computer Multilayer Board Layout			F
257	Redesign of Rope and Erasable Memory Drivers			F
258	Redesign of Computer Power Supply Module			F

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
259	Redesign of Computer Erasable Memory			F
291	Redesign of DSKY Alarm Lights			F
324	Computer Sense Amplifier Change			F
351	Modify Computer Alarm Module			F
402	Computer Clear Driver Circuit Modification			F
403	Computer Strobe Adjustment			F
460	Addition of Jumper Wires in Tray A of Computer			F
176	Computer Module Vibration			H
263	PSA Helicoil Change			H
296	Cementing Relay Assembly			H
301	Thermal Instrumentation			H
316	PSA and PTA Header Change			H
318	Corrosion Protection of Exposed Beryllium			H
320	Edge Blackening of AOT Lenses			H
322	Computer Wiring Changes			H
336	Change CDU Potting Material			H

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
353	Change AOT Pressure Seal Material			H
355	IRIG Change			H
367	Addition of Light Diffusing Paint to DSKY			H
368	Improved Computer Power Supply Module Relays			H
419	DSKY Indicator Drive Module Relay Replacement			H
440	"Clear Rope" Driver Circuit Modification	0104101	8104209	H
443	Replacement of Computer Screws			H
447	Replacement of Plastic Pads under Computer Tray A and B Covers	0104101	8104209	H
452	Computer Wiring Changes to Accommodate Auxiliary Memory Unit			H
454	AOT Pinning			H
461	Replacement of Diodes in Gimbal Servo Amplifier	0102666	8102696 8102707	H
462	Addition of Ground Strap to LEM Nav Base	0102668	8102701	H
470	Random Workmanship Vibration			H

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
474	Computer Test Connector Jumpers	0104113	8104221	H
476	Painting of DSKY Alarm Indicator Face			H
478	Painting of Exposed Surfaces on Computer Mid-Tray Spacer			H
479	DSKY Teflon Coated Push-button Shaft			H
485	Redesign Computer Power Supply			H
486	Cut Pins on Computer Power Supply	0104104	8104212	H
489	Replacement of Transformers in LEM ECDU			H
493	DSKY Y-Line Feedback Base Resistor Change			H
494	DSKY Wiring Improvement			H
499	Addition of ECDU Damper Plate		8102712 8102719	H
500	Replacement of Capacitor in PIPA Preamplifier	0102681	8102717 8102715 8102716 8102713	H
501	Implementation of Flight Processing Spec ND-1002313			H
515	Replacement of Resistors in ECDU CSA			H

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
518	Standby Change on Computer			H
533	Addition of Uplink Wires in A Harness		8102726	H
483	Correction of Sense Amplifier Breakdown			J
505	Implementation of Flight Processing Spec ND-1002341 and New Diode			J
511	Correction of Computer Noise SCAFAL Problem			J
148	CDU Transformer Change			K
173	Reticle Mount and Objective Lense Assembly			K
179	G and N Filter Change			K
191	CDU Electronics Module Change			K
217	Delete Signal Conditioner Power Supply Assembly			K
221	Z Axis Irig Rotation			K
307	Middle Axis Assembly Clamp Changes			K
308	Stable Member Heat Transfer Change			K
309	PIP Temperature Deviation Reduction and Temperature Alarm Test			K

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
310	IMU Cross Coupling change			K
359	Replacement of IMU Mounting Bolts	0102643	8102668	K
505	Implementation of Flight Processing Specification ND1002314 and New Diode			K
302	Manufacture of Block II and LEM Signal Conditioner Assemblies			L
538	Replacement of CCRD Reticle Brightness Potentiometer			L
558	Replacement of Mounting Hardware in LGC Installation Kit	0104120		L
358	Redesign of AGC Handling Fixture	0104096	8104172	M
506	Modification of AGC Handling Fixture (Block II)			M
509	AGC/GSE Compatibility	0104107	8104215	M
512	AOT High Density Filter Assembly			M
539	AOT Reticle Lamp Change		8106058	M
540	AOT Reticle Knob Change		8106058	M
542	AOT Eyeguard Plug		8106058	M
543	AOT Counter Moisture Proofing and Illumination		8106058	M

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
562	Replacement of LM-1 Harness Lacing Tape			M
585	PIP Preamplifier Capacitor Replacement		8102733 8102734	M
594	CCRD Aluminum Overlay		8102738 8102735 8102729	M
605	IMU Blanket Removal	0102687 0102688	8102733 8102734	M
603	Capacitor Replacement in CDU MSA and Quadrature Rejection Module		8102744 8102746	R
609	Elimination of CDU DAC Saturation during coarse align		8102744 8102746	R
577	Addition of Diode to LEM PSAAM's			S
582	LTA-8 Modifications			S
587	IRIG Gyro End Cap Replacement			S
596	LM-2 Modifications			S
618	LM-3 Modifications			S
622	Non-metallic materials Flammability Modification for PSA	0102690	8102754	S
624	Non-metallic materials Flammability Modification for SCA	0102691	8102749	S
626	Modification of LEM Harness Group for Flammability Protection	0102692	8102751	S

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
564	Implementation of Flat Pack Specifications ND 1002359A and ND 1002358B			U
631	Replace RTV-102 with RTV-109	0102679 0102689 0102690	8102752 8102755 8102754 8102766	U
653	Modification of IMU Wiring to Reduce IRIG Pre-Amp Oscillation		8102763	U
641	Non-metallic Materials Modification for DSKY	0104126	8104241	W
655	New LGC Mounting Bolts and Spacers			W
673	Redesign of DSKY Push-button Cap Housing Assembly Leaf Spring	0104126	8104241	W
678	IRIG End Cap Change	0102697	8102767 8102768	W
633	AOT Pressure Seal Protection and Other Flammability Fixes	0106049 0106048	8106069 8106073	Y
604	Incorporation of E-memory Vibration Pads			Z
688	Modification of IMU to Reduce Sporadic Oscillation of IRIG Preamps		8102773 8102774	Z
657	Conical Sunshade and Radar Shield Assembly for AOT	0106050	8106076	AC
697	AOT Harness Protective Shield	0106054	8106085	AC

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
719	Computer Alarm Module Modification, V-Fail Detection	0104132	8104248	AD
735	DSKY IL and EL Safety Glass Fix	0104135	8104251	AD
743	New Configuration of Installation Kit			AD
757	Design Changes to Correct LEM PSA Reverse Power Problem			AE
768	DSKY EL thermal/ Vacuum Screen modification	0104138	8103954	AG
739	Addition of 4 lights on DSKY indicator panel	0104136	8103952	AG
780	Taping of AOT cable			AG
781	ECDU mounting bolt change in length	0102703	8102789	AG
815	Replace AGC Connector Assembly with a restart monitor	0102705	8102793	AH
1017 & 1032	Replace blower motor in IMU to increase reliability	-	8102796	AJ
1030	Replace ECDU modules containing 1010274 transformers to increase reliability	-	-	AJ

WARNING AND CAUTION PAGE

The following warnings and cautions apply to the system for which this manual was written. These warnings and cautions must be observed to avoid personal injury and/or equipment damage.

CHEMICAL HAZARDS

WARNING

Beryllium is a highly toxic metal. Processes such as deburring, machining, or grinding of beryllium, if expressly authorized, as well as other procedures that produce airborne beryllium particles, should be performed with local exhaust ventilation which is connected with an acceptable exhaust-filtration system. The inhalation of airborne beryllium particles can cause serious respiratory disability. All injuries where the skin is damaged, including puncture wounds and skin rashes, should be reported immediately so that proper treatment measures can be taken. Air in these areas should be monitored to insure that the amount of airborne beryllium remains below the established threshold limit value.

CAUTION: Wear nylon gloves or finger cots while handling beryllium parts unless parts are to be immediately cleaned after handling. Moisture and oils from the skin have a highly corrosive effect on beryllium.

WARNING AND CAUTION PAGE (Continued)

WARNING

When using equipment containing mercury (i.e. battery power pack; auxiliary battery pack; differential voltmeter, Fluke 803B), avoid spilling mercury. Mercury is a toxic metal and may contaminate equipment, clothing, and body. After use of such equipment, visually inspect area and equipment to verify absence of mercury. If mercury contamination exists, see mercury use guide lines (page I-xxxivB).

WARNING

Do not leave mercury in open containers. Keep in tightly closed unbreakable container when not in use, since mercury vapor is toxic.

CAUTION: Avoid spilling mercury from open mercury pool. Liquid or vaporous mercury can cause severe corrosion and/or cracking of unprotected aluminum and other non-ferrous metals. If mercury contamination of equipment exists, report to AC Electronics site manager and site quality control representative.

WARNING AND CAUTION PAGE (Continued)

WARNING

Wear goggles, rubber gloves, and rubber aprons when working with acid solutions. Do not spatter solution. If acid contacts skin or eyes, immediately flush affected area with mild boric acid solution or water and report to nearest medical facility.

WARNING

Do not spatter battery cell electrolyte. If electrolyte contacts skin or eyes, immediately wash affected area with mild boric acid solution or water and report to nearest medical facility.

CAUTION: Always add acid to water; do not pour water into acid. Equipment surface can be damaged from uncontrolled chemical reaction. However, distilled water, if required, may be slowly added to replenish the electrolyte of a battery.

CAUTION: Keep battery cells upright, unless otherwise noted, to prevent loss of electrolyte.

WARNING AND CAUTION PAGE (Continued)

CAUTION: Add only distilled water to nickel cadmium battery cells. Never add acid or use instruments that have been used to fill lead acid batteries. Acid will damage the plates of the nickel cadmium cells.

CAUTION: Prevent acid from contacting painted surfaces. Immediately wipe off any acid on a painted surface, since prolonged contact will cause damage.

ELECTRICAL HAZARDS

WARNING

Use extreme care when reaching inside the G and N coolant and power console. Lethal voltages exist at power line filters and at the power and signal input panel.

WARNING

Always use moisture-proofing protection (covers, rubber seals, gaskets, and sealing compound) for PSA connectors and pins not secured to mating connectors. Otherwise, connector and pin corrosion may cause short circuits.

CAUTION: Maintain IMU heater power at all times, except during use of IMU shipping container, to prevent damage to IMU.

CAUTION: Handle G and N harnesses with care to avoid damage to connectors, conductor wires, and/or potting.

CAUTION: Turn off equipment when any power connections are being made to prevent pin damage due to arcing.

WARNING AND CAUTION PAGE (Continued)

CAUTION: Exercise extreme care when removing and installing electrical connectors. Visually check all pins for straightness. Where applicable, use special gages and reticles to check pin alignment during connector removal or installation. Install or remove connectors with jack screws by turning each screw one turn at a time to maintain parallelism between plug and connector during entire operation. Otherwise, bent pins can cause short circuits and additional equipment damage.

MECHANICAL HAZARDS

WARNING

Do not extend any equipment cabinet drawer slides until drawers are to be installed. The extended slides can cause serious injury to personnel.

WARNING

Do not extend more than one cabinet drawer at a time. Extension of more than one drawer at a time can cause console to topple, endangering personnel and equipment.

OPTICAL HAZARDS

CAUTION: Always keep lens covers on optical equipment when it is not in use to protect optically ground and coated surfaces from damage.

WARNING AND CAUTION PAGE (Continued)

MERCURY USE GUIDE LINES

A. Mercury is volatile at room temperature, and mercury and mercury vapors are toxic. If mercury is accidentally spilled, avoid further contamination using the following methods:

   (1) Ventilate area with fans or other suitable means during clean-up.

   (2) Clean up major portion of spill.

B. Avoid prolonged or repeated contact with skin.

C. Wash hands thoroughly with soap and warm (not hot) water before eating or smoking.

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Chapter 1

SYSTEM TIE-IN

1-1 SCOPE

This chapter presents the lunar excursion module (LEM) mission. The chapter also describes the functional interface between the primary guidance, navigation, and control system (PGNCS) and the other spacecraft systems.

1-2 LEM MISSION

The purpose of the LEM mission is to transfer the LEM from a circular lunar orbit into a descent orbit, land two astronauts on the lunar surface, and return them to the orbiting command and service module (CSM). The LEM mission (figure 1-2), with respect to the PGNCS, is best described by dividing it into six phases: separation and transfer orbit insertion, descent coast, powered descent and landing, lunar stay, launch and powered ascent, and rendezvous and docking.

1-2.1 SEPARATION AND TRANSFER ORBIT INSERTION. Approximately one hour before the LEM enters the descent orbit, two astronauts leave the CSM and enter the LEM through the top docking hatch. The crew then checks out the various LEM systems, establishes a voice link, and, after initial PGNCS turnon, establishes a time reference for the LEM guidance computer (LGC), and coarse aligns the inertial measuring unit (IMU) using CSM data. One astronaut then manually commands reaction control system (RCS) jet firing to separate the LEM from the CSM. The IMU is fine aligned. Near the end of the second lunar orbit, the LEM descent engine is fired by the PGNCS and the LEM begins its descent. The timing and duration of LEM descent engine firing is critical, to insure the proper elliptical Hohmann transfer orbit.

1-2.2 DESCENT COAST. During the descent coast phase, the LEM is in free fall on an elliptical flight path. During free fall, the astronauts check out the landing radar (LR). At the perilune of the Hohmann transfer orbit, the LEM is at an altitude of approximately 50,000 feet and has a velocity vector essentially parallel to the lunar surface. During this phase, the PGNCS determines the flight parameters required for powered descent. The rendezvous radar (RR) tracks its transponder in the orbiting CSM and provides the LGC with updated information on the position of the CSM.

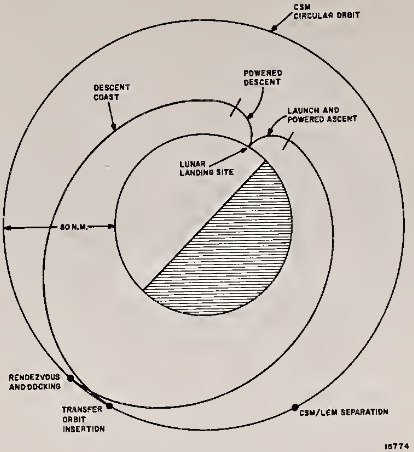


Figure 1-2. LEM Mission Phases

1-2.3 POWERED DESCENT AND LANDING. In preparation for powered descent, an IMU fine alignment is performed. At the perilune of the descent orbit, the PGNCS issues a descent engine start discrete. The descent engine firing slows the LEM which begins the actual descent to the lunar surface. During descent, the PGNCS controls the engine trim and thrust level, controls the LEM attitude, and provides visual displays of the guidance system status. During the final approach and landing, the PGNCS holds the LEM at a constant attitude, allowing the astronaut to view the landing site. The astronaut can select a new landing site by inserting new landing site coordinates into the LGC. The LGC will automatically control the RCS and the descent engine to guide the LEM to the new landing site. Inertially derived flight parameters are updated in the LGC by comparison with the altitude and velocity parameters determined from LR measurements.

1-2.4 LUNAR STAY. After LEM touchdown the astronauts check out all systems for damage and insure that the systems can perform the functions required for a successful ascent. All equipment not required for lunar stay is then turned off. The astronauts survey the surrounding lunar landscape, secure the hatches, and perform a final check on the portable life support system (PLSS). After the LEM is secured, one astronaut, wearing the PLSS, leaves the LEM to explore the lunar surface. The exploring astronaut inspects the LEM and sets up communication antennas. A television system sends pictures of the lunar scene to earth. The astronaut, always in direct voice contact with the LEM, explores the lunar surface, makes photographic records, and collects surface samples. After approximately three hours, the astronaut must return to replenish his PLSS. Additional surface explorations depend upon the planned stay time. Near the end of the lunar stay, the PGNCS is brought to an operate condition and the IMU is coarse and fine aligned. The IMU is fine aligned to a known reference coordinate system by making star sighting measurements with the alignment optical telescope (AOT). RR tracks its transponder in the orbiting CSM and sends data to the LGC which calculates applicable flight parameters in preparation for the launch and power ascent.

1-2.5 LAUNCH AND POWERED ASCENT. After the astronauts prepare the LEM, the PGNCS determines time of launch and ascent trajectory based on a fixed rendezvous aim point. Mechanical and electrical separation of the two LEM stages takes place and the LGC issues the ascent engine start discrete at a time calculated to effect a successful rendezvous.

During powered ascent, the LEM rises vertically and then is pitched to attain a Hohmann transfer orbit for the rendezvous. Because the ascent engine is a fixed-position, fixed-thrust engine, the LEM attitude during ascent is controlled by the LGC which issues commands to the RCS jets. The LGC determines necessary RCS commands by comparing calculated values with actual flight parameters obtained from the inertial subsystem (ISS), and determines required attitude changes to correct any differences. When the injection of the LEM into the proper elliptical orbit is accomplished, the LGC issues the ascent engine off discrete and the LEM enters the coasting portion of the ascent phase.

1-2.6 RENDEZVOUS AND DOCKING. LEM guidance during this phase is a combination of radar tracking data and inertial data. Shaft and trunnion data from the RR and velocity and attitude information from the IMU are used by the LGC to control the RCS to maintain attitude and to provide a display of position and velocity information. During rendezvous, the LEM is maintained at an orientation such that the CSM is visible through the vehicle windows.

Terminal rendezvous maneuvers begin when the LEM and CSM are approximately five nautical miles apart. The LGC computes the intercept time and with this data updates the thrust vector and velocity requirements. Three ascent engine burns during terminal rendezvous reduce the closing rate to near zero. The LGC utilizes the RCS to maintain vehicle attitude during these burns. The final step is docking, which is initiated when the vehicles are approximately 500 yards apart. The astronaut uses the translation controller and attitude controller in a computer-aided manual operation to guide the LEM to hard docking with the CSM. The two astronauts then leave the LEM and transfer to the CSM through the vehicle's upper tunnel to prepare for the return to earth. The LEM is jettisoned following crew transfer to the CSM.

1-3 LEM STRUCTURE

The LEM (figure 1-3) has two stages mated to form one structure: the ascent stage and the descent stage. These stages and the umbilical interconnecting cables can be separated at launch from the lunar surface or because of mission abort during descent.

The approximate LEM external dimensions are shown in figure 1-4. At earth launch, the weight of the LEM is approximately 30,000 pounds.

1-3.1 ASCENT STAGE. The ascent stage, constructed mainly of aluminum alloy, consists of the crew compartment, a midsection, aft equipment bay, tankage sections, associated hatches, and windows.

From the crew compartment, the astronauts control all phases of the LEM mission. The crew also uses this compartment as their operations center during their lunar stay.

The displays and controls associated with the PGNCS are located at the front of the crew compartment. The IMU, a portion of its electronics, and the AOT are located in an enclosure above the crew compartment. The remaining PGNCS components are mounted on coldplates to the rear wall of the ascent stage midsection.

The midsection is cylindrical, smaller than the crew compartment, and directly behind it. The ascent engine and related components are in the midsection, the LEM's center of gravity. Also contained in the LEM's midsection are the ascent engine hatch, top hatch, environmental control system (ECS), and equipment that requires crew accessibility.

To transfer from the CSM to the LEM while in lunar orbit, the crew uses the upper docking tunnel at the top centerline of the ascent stage. The forward tunnel, at the lower front of the crew compartment, is used for entering and leaving the LEM while on the lunar surface.

The aft equipment bay, at the rear of the vehicle, is separated from the midsection by a pressure-tight bulkhead. This area houses the glycol loop for the ECS, inverters, batteries, and equipment for the electrical power system (EPS).

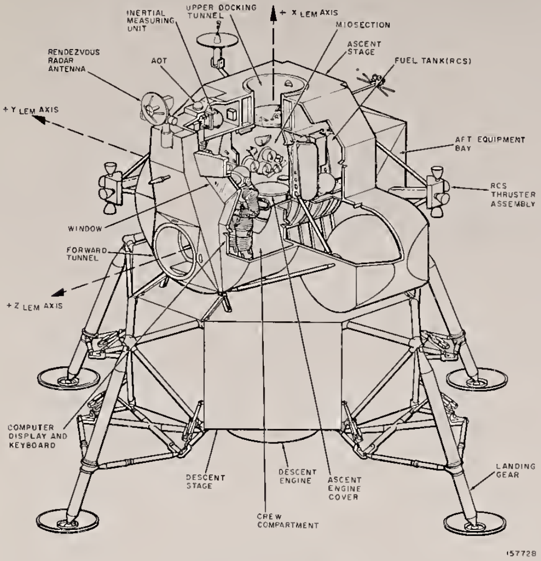


Figure 1-3. LEM

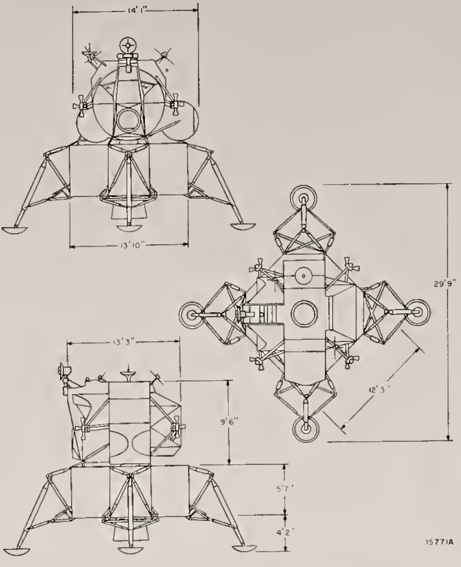


Figure 1-4. LEM External Dimensions

The propellant tankage sections are located on either side of the midsection outside the pressurized area. The tankage sections contain the ascent engine fuel and oxidizer tanks; RCS fuel, oxidizer, and helium tanks; and ECS water tanks. The ratio by weight of oxidizer to fuel is 1.6 to 1; therefore, to maintain the lateral center of gravity on the vehicle X axis, the ascent engine propellant tanks are offset to one side.

Two triangular windows in the front face of the crew compartment provide visibility. Each window has approximately 1.6 square feet of viewing area and are canted down and to the side to increase visibility. Each window consists of two panes.

1-3.2 DESCENT STAGE. The descent stage, constructed mainly of aluminum alloy, has equipment necessary to land on the lunar surface. It is also a platform for the launching of the ascent stage after completion of the lunar exploration. The descent engine is the center of the stage surrounded by its four main propellant tanks. In addition to the descent engine and its related components, the descent stage houses the descent control instrumentation; scientific equipment; EPS batteries; and tanks for water used by the ECS. Landing gear and the LR antenna are attached to the descent stage.

1-4 LEM SYSTEMS

Functionally, there are seven LEM systems. Four of these systems control the LEM flight. The PGNCS or the stabilization and control system (SCS) receives inputs from the crew and electrical inputs from the inertial sensors to generate commands that result in rotation and translation maneuvers. The RCS or propulsion system provides external forces and mechanical couples to maneuver the LEM under the control of the PGNCS or the SCS. The crew obtains information from the LGC (part of the PGNCS), by communications (Manned Space Flight Network), or displays that indicate the necessity to initiate one or more of the basic LEM motions. The three remaining LEM systems are indirectly related to LEM control. They provide the power (EPS), environmental control (ECS), and the communications [communications and instrumentation system (CIS)].

1-4.1 PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM. The PGNCS provides the measuring and data processing capabilities and control functions necessary to accomplish the LEM mission. The PGNCS utilizes inertial components for guidance, an optical device and radar for navigation, and a digital computer for data processing and issuance of flight control signals.

The inertial guidance portion of the PGNCS, the IMU, employs accelerometers mounted on a gyroscopically stabilized gimbal-mounted platform. The IMU senses acceleration and attitude changes instantaneously and provides signals to a digital computer, the LGC, for the generation of attitude control and thrust commands.

For navigation, the PGNCS utilizes the AOT to take star sightings and obtain measurements. These sightings are used by the LGC to establish proper alignment of the stable platform. The LGC contains a catalog of celestial bodies and is programmed to calculate alignment commands using the information obtained from the optical sightings. During descent, altitude and velocity information from the LR is used to update inertially derived data. During the coasting descent, lunar stay, and rendezvous phases of the mission, the RR tracks its transponder in the orbiting CSM to provide range, range rate, and antenna angle measurements to the LGC. In addition to functioning as a data processing unit, the LGC, through its flight programs, performs the function of a digital autopilot in controlling the LEM.

1-4.2 STABILIZATION AND CONTROL SYSTEM. The SCS consists of two major sections: the control electronics section (CES) and the abort guidance section (AGS). The CES processes flight control signals during all mission phases. The AGS provides the CES automatic steering commands, derived from explicit guidance equations, in the event of mission abort due to a PGNCS malfunction.

The CES consists of an attitude and translation control assembly (ATCA), a descent engine control assembly (DECA), rate gyro assembly (RGA), two translation controller assemblies (TCA), and two attitude controller assemblies (ACA). The CES processes and routes signals to fire any combination of the 16 thrusters in the RCS to control LEM attitude and translation. The attitude and translational control inputs originate from any of three sources: the PGNCS during normal automatic operation, the ACA and TCA during manual operations, or the AGS during an abort.

The CES converts the applicable input commands into pulsed or constant level signals and routes them to the RCS to fire the appropriate thrusters. Rate signals from the CES are displayed on the flight director attitude indicator (FDAI).

The CES also processes "ON-OFF" commands for the ascent and descent engines, and routes automatic and manual throttle commands to the descent engine. Trim control of the descent engine insures that the thrust vector operates through the vehicle center of gravity.

The AGS provides abort capability from any point in powered descent or powered ascent and increases crew safety by acting as a backup system to the PGNCS. This backup guidance provides vehicle attitude, angular velocity, and translational acceleration indications. The AGS has three main assemblies: abort sensor assembly (ASA), abort electronics assembly, and data entry and display assembly.

The ASA utilizes a strap-down technique employing three single-degree-of-freedom integrating rate gyros and three accelerometers. It is mounted to the PGNCS navigation base on the same mounting pads as the AOT. The outputs of the abort sensor assembly go to the abort electronics assembly, a 4,096 word capacity general purpose computer. Computations are performed using the inputs from the abort sensor assembly. When the AGS is in control of the LEM, the results are displayed and control signals are issued to the vehicle's reaction control and propulsion systems.

The abort sensor assembly measures the accelerometer triad rotation from, and resolves the acceleration into, a fixed reference frame. This reference frame is provided by an initial alignment of the AGS with the PGNCS. Initial alignment is required for attitude, velocity, time, and position. Velocity and position vectors are manually entered into the computer by a data entry device available to the astronaut.

Attitude alignment is accomplished by transferring PGNCS IMU gimbal angles to the computer. The abort electronics assembly receives this data from the coupling data unit (CDU) in the same manner and at the same time as the LGC (i.e. incremental angles accumulated from a zero reference after "CDU ZERO").

1-4.3 PROPULSION SYSTEM. The LEM utilizes separate, complete, and independent descent and ascent propulsion systems, which consist basically of a liquid propellant rocket engine and its propellant storage, pressurization, and feed components.

The descent propulsion system is in the LEM descent stage and utilizes a throttle-controlled, gimbaled engine. The engine injects the LEM into the descent transfer orbit and is used during powered descent and landing to control the rate of descent. The descent engine, developing 10,500 pounds maximum thrust in a vacuum at full throttle and 1,050 pounds minimum thrust, can be gimbaled 6 degrees in any direction. The PGNCS issues the "ON-OFF" commands for the descent engine and also provides signals controlling thrust magnitude and gimbal trim position.

The propellant used in both propulsion systems is a 50-50 fuel mixture of hydrazine and unsymmetrical dimethylhydrazine using nitrogen tetroxide as the oxidizer and helium as the tank pressurant.

The ascent propulsion system utilizes a fixed, constant-thrust engine installed along the centerline of the ascent stage midsection and includes the associated propellant feed tanks and pressurization components. The engine develops 3,500 pounds thrust in a vacuum, sufficient to launch the ascent stage from the lunar surface and place it in orbit. The PGNCS issues the "ON-OFF" commands for the ascent engine.

1-4.4 REACTION CONTROL SYSTEM. The RCS provides rocket thrust impulses that stabilize the LEM during descent and ascent and control the LEM attitude and translation about or along all axes. The RCS has 16 thrust chambers supplied by two separate and independent propellant feed and pressurization sections. The thrust chambers are mounted in clusters of four on outriggers equally spaced around the LEM ascent stage. In each cluster, two thrust chambers are mounted on a vertical axis, facing in opposite directions; the other two are spaced 90 degrees apart, parallel to the LEM's Y and Z axes. The RCS utilizes the same fuel as the ascent engine. In the event of RCS fuel depletion, the remaining ascent fuel can be used for the RCS. The RCS can be operated in any of three modes: manual, automatic, or semi-automatic. The PGNCS supplies "ON-OFF" signals through the SCS to the valves on the desired thrust chambers during the automatic or semi-automatic mode. The automatic mode is normally used to provide attitude control during all mission phases except when manual control is required. It is possible to select manual control in one or two axes and retain automatic control in the other axis during all mission phases. The semiautomatic mode combines automatic attitude hold control with manual control. The LEM attitude is changeable about each axis using the astronaut's attitude controller. This mode is used primarily to control the LEM during the rendezvous and docking phase of the mission. In the manual mode, all control commands originate from the attitude controller, including manual control of the thrust duration.

All automatic translational commands originate in the PGNCS and are routed to the RCS similar to the attitude control signals.

1-4.5 ELECTRICAL POWER SYSTEM. The EPS provides 28 vdc and 115 vac, 400 cps power to the PGNCS. This power originates from six batteries, four in the descent stage, and two in the ascent stage. The batteries, the silver-zinc type, are rated at 80 watts per hour per pound of weight. The 115 vac, 400 cps power is obtained by routing the 28 vdc through an inverter.

1-4.6 ENVIRONMENTAL CONTROL SYSTEM. The ECS sustains life in space by providing breathable atmosphere, acceptable temperatures, food and water, and waste disposal. In addition, the ECS circulates an ethylene glycol-water coolant about the temperature sensitive electronic equipment in the PGNCS and other LEM systems to provide thermal stability. The IMU has coolant circulated through its case while the power and servo assembly (PSA), pulse torque assembly (PTA), signal conditioner, LGC and CDU are mounted on coldplates through which the coolant is circulated to provide temperature control.

1-4.7 COMMUNICATIONS AND INSTRUMENTATION SYSTEM. The CIS links the lunar astronauts, the orbiting CSM, and earth monitoring stations.

The communications portion contains two radio frequency (RF) sections, one operating in the VHF range and the other in the UHF range; a television section; and a signal processing section. In addition to two-way voice communication, the RF section receives and transmits tracking and range information, biomedical information, and emergency code keying in the event of voice transmission failure. The television section is used by the extravehicular astronaut to televise the lunar surface within an eighty foot radius of the grounded LEM. In the signal processing section, critical signals of the PGNCS are conditioned and supplied to pulse code modulated (PCM) telemetry equipment for transmission to earth. Telemetry data can be stored when direct communication with the earth is not possible.

The instrumentation portion provides the astronauts and ground facilities with LEM performance data during the mission by sensing physical status data, monitoring the various systems, and performing inflight and lunar surface checkout. This system also contains the scientific instruments which are used by the astronauts during their lunar stay.

1-5 PGNCS INTERFACE

PGNCS operation during the LEM mission requires the interface of the PGNCS with the other LEM systems, the displays and controls on the crew display and control panels, the RR, the LR, and the astronauts. The functional interface of the PGNCS is shown in figure 1-5.

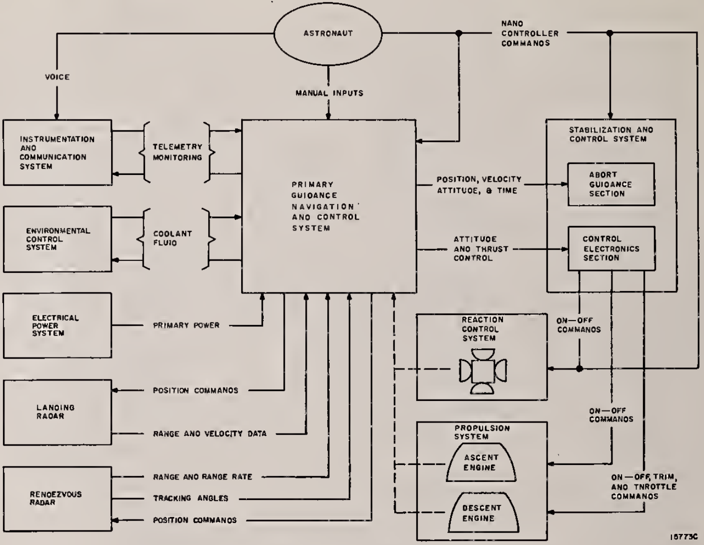


Figure 1-5. LEM PGNCS Functional Interface, Block Diagram

1-5.1 SYSTEMS. Four LEM systems (SCS, ECS, CIS, and EPS) have direct interface with the PGNCS and two systems (propulsion system and RCS) have indirect interface with the PGNCS. The indirect interface of the propulsion system and the RCS occurs through the SCS. These two systems may thus be controlled by the PGNCS or by the backup control provided by the AGS of the SCS. Descriptions and sources of the SCS interface signals are provided in table 1-I. Descriptions of the interfaces with the other systems are provided in paragraph 1-4.

1-5.2 DISPLAYS AND CONTROLS. Several displays and controls located on the crew control panels, LGC display and keyboard (DSKY) panel, and the SCS control panel interface with the PGNCS. Two sets of hand controllers are provided for manual control of the LEM and interface with the PGNCS. Descriptions of the displays and controls are in table 1-II.

1-5.3 LANDING RADAR. The landing radar (LR) provides data to the LGC from which LEM velocity (in antenna coordinates) and LEM altitude may be determined. The data is also available for visual display, independent of the PGNCS, except that the velocity is in spacecraft coordinates.

The landing radar which operates in the X-band, consists of an antenna assembly, a solid-state electronics assembly, and a control panel. Velocity data is acquired from a three beam continuous wave Doppler radar. Altitude data is provided by a one beam FM continuous wave radar altimeter. The antenna assembly accommodates the requirements of both the Doppler and the altimeter beams.

Landing radar and PGNCS interface include digital data transfer, scaling, velocity and range sensing, status, and antenna positioning. Descriptions and sources of the interface signals are in table 1-III.

1-5.4 RENDEZVOUS RADAR/TRANSPONDER. The rendezvous radar/transponder (RR/T) provides range, range rate, and angle data to the LGC to enable computation of a trajectory from the moon to a point in space where the final docking of the LEM to the CSM can begin. Outputs from the RR are also available for visual display.

When the LEM is on the lunar surface, the RR tracks the associated transponder in the CSM to furnish updated information to the LGC. During the LEM ascent coasting phases, the RR is used for monitoring or midcourse correction maneuvers. During automatic operation of the RR, the RR is controlled by inputs from the LGC. The astronauts can manually control the RR with controls and indicators located on the radar panel of the commander's lower console.

The RR consists of an antenna assembly and an electronics assembly. The antenna assembly contains the microwave radiating and gimballing elements and internally mounted gyros, resolvers, multiplier chains, modulators, and mixer preamplifiers.

The antenna is a four horn, amplitude comparison, monopulse type which uses a Cassegrainian configuration to minimize the total antenna depth. Components are distributed inside the antenna to achieve balance around each axis. Each axis (shaft and trunnion) is controlled by a brushless servo motor driven by pulse width modulated drive signals. The antenna transmits and receives circular polarized radiation to minimize signal variations resulting from attitude changes of the linearly polarized transponder antenna.

Four rate integrating gyros are used for line of sight (LOS) space stabilization and LOS angle rate measurement. Only two of the gyros are used at any one time; if either of the two gyros fail, a logic circuit transfers control to the other two gyros. A two speed resolver is mounted on each axis for antenna angle data required by the LGC and for display. The multiplier chain supplies X-band power for radiation and for local oscillator excitation. The modulator provides phase modulation of the X-band carrier.

The electronics assembly contains the antenna control amplifiers, range tracker, frequency tracker, frequency synthesizer, receiver, and signal data converter.

Shaft and trunnion positioning signals from the CDU are converted into dc error signals by the antenna control amplifiers. The dc error signals are used to torque the antenna gyros and produce gyro output error signals. The gyro error signals cause the antenna servo loop to drive the antenna to the commanded positions.

The range tracker operates with the transponder and uses a multitone ranging system. The RR transmission is phase modulated with sine wave, 200 cps, 6.4 kc, and 204.8 kc tones. By comparing the phase of the received 200 cps tone with the transmitted 200 cps tone, range measurements from 0 to 390 miles can be made. Similar phase comparisons made with the 6.4 and 204.8 kc tones provide successive refinements of ranging accuracy. The lower frequency tone is used for coarse range extraction; the higher frequency tones provide fine range data.

The frequency tracker nulls through the band of expected received Doppler frequencies and provides an output which represents range rate.

The frequency synthesizer generates all of the fixed frequencies required for coherent signal transmission and reception. A single 1.7 mc stable crystal oscillator and a system of multiplication, division, and mixing is used to produce the required frequencies.

The receiver is a highly stable, three channel, triple conversion superheterodyne. Two channels are provided for the shaft and trunnion signals and one channel is provided to amplify the sum or reference signal.

The signal data converter provides the interfaces between the RR and the LGC. The signal data converter contains a computer interface unit and an input-output amplifier. The computer interface unit processes the radar output signals into the format required by the LGC. The processed signals are then selected sequentially for transfer to the LGC by coded strobe signals provided by the LGC. Control and status discretes are routed to the LGC through the input-output amplifier. The input-output amplifier also routes control and status signals to and from the LEM controls and displays.

The transponder consists essentially of a triggered frequency-shifting transmitter. The purpose of the transponder is to extend the range of the low power radar by decreasing losses.

Table 1-I. SCS Interface Signals

Signal Name	Source	Description
Manual translation commands (±x, ±y, ±z)	SCS	Signals from translation controller which fire RCS jets by LGC control.
Attitude control out of detent	SCS	Signal from attitude controller indicating that it is not in neutral position.
Rate of descent (±)	SCS	Discretes commanding an increase or decrease in rate of descent.
Gimbal off (pitch, roll)	SCS	Signal to LGC indicating that descent engine pitch or roll gimbal is off null.
Trim commands (± pitch, ± roll)	LGC	Signals which control trim of descent engine.
Engine on-off	LGC	Signal to turn descent or ascent engine on or off.
Descent engine throttle command (decrease, increase)	LGC	Signal to increase or decrease thrust of descent engine.
RCS jets on-off	LGC	Signals (16) to turn RCS jets on or off.
Increments of 1MU gimbal angles ($\pm\angle\theta_{1G}$, $\pm\Delta\theta_{MG}$, $\pm\angle\theta_{OG}$	LGC	Supplies changes in 1MU gimbal angles to AGS.
CDU zero (initial clear)	LGC	Sets alignment logic of AGS to zero.
800 cps ±1%	PGNCS	Provides reference between PGNCS and SCS.

Table 1-II. Displays and Controls

Display or Control	Function
GUID CONT switch	Selects either primary guidance (PGNS) or abort guidance (AGS). Normally in the PGNS position.
MODE SEL selector	Three position switch used during landing phase to select one of three inputs to be displayed on AZ RT/ELEV RT-LAT VEL/FWD VEL indicator. Inputs are landing radar (LDG RADAR), PGNS and AGS.
RNG/ALT MON switch	Controls display of RANGE/RANGE RATE-ALT/ALT RATE indicator. Positions are RNG/RNG RT and ALT/ALT RT.
RATE/ERR MONITOR switch (2)	Selects one of two inputs for AZ RT/ELEV RT-LAT VEL/FWD VEL indicator and attitude needles of FDAI.
ATTITUDE MON switch (2)	Selects one of two inputs to FDAI total attitude display and attitude error needles during landing.
THR CONT switch	Selects either automatic (AUTO) or manual (MAN) control of descent engine throttle. Normally in AUTO position.
MAN THROT switch	Activates either commander's (CDR) or system engineer's (SE) translation controller for manual throttling of descent engine.
ABORT	Pushbutton to cause mission abort at any point between LEM/CSM separation and touchdown on lunar surface with descent stage still attached.
ABORT STAGE	Pushbutton to cause mission abort using ascent stage.
AZ RT/ELEV RT-LAT VEL/FWD VEL meter (2)	Provides visual displays of vehicle forward and lateral velocity during landing.

(Sheet 1 of 2)

Table 1-II. Displays and Controls

Display or Control	Function
RANGE/RANGE RATE- ALT/ALT RATE meter	Provides visual displays of range, altitude, range rate, and altitude rate.
FDAI meter (2)	Provides three visual displays, total attitude, attitude error, and attitude change rate. PGNCS or AGS provides inputs for total attitude and attitude error. Attitude rate signals are provided by SCS rate gyros.
LGC and ISS warning indicators, PGNS caution indicator.	Controlled by instrumentation system which receives discretes from LGC when certain PGNCS troubles exist.
MODE CONTROL selector	A three-position selector located on SCS control panel concerned with attitude control. Positions are OFF, ATT HOLD, and AUTO. In AUTO position, fully automatic attitude control is achieved through PGNCS or AGS control of RCS jets. ATT HOLD position allows crew to manually reposition LEM and have new position automatically maintained by LGC.
IMU CAGE switch	Switch located on DSKY mounting panel to drive IMU gimbal angles to zero.
Attitude controller (2)	Three-axis, pistol-grip, right-hand device for manual attitude control of LEM. Outputs from controller are processed by PGNCS or may be routed directly to RCS.
Translation controller (2)	Three-axis, T-handle, left-hand device for manual translation control of LEM. Using switch located next to T-handle, controller can operate RCS jets or throttle the descent engine.

(Sheet 2 of 2)

Table 1-III. Description of Landing Radar Interface Signals

Signal Name	Source	Description
Antenna positioning command	DSKY and LGC	Changes antenna position.
Antenna position #1 (descent)	LR	Indicates to LGC that antenna is in position #1.
Antenna position #2 (hover)	LR	Indicates to LGC that antenna is in position #2.
Velocity data good	LR	Indicates to LGC that LR velocity trackers have locked on.
Range data good	LR	Indicates to LGC that LR range trackers have locked on.
Range low scale factor	LR	Indicates to LGC that a change in scale factor is necessary. Issued automatically at approximately 2,500 feet.
LR in "0" and LR in "1"	LR	Digital pulses sent to LGC which contain range and velocity data.
Readout command	LGC	Indicates that LGC is ready to receive LR data pulses.
Gate reset	LGC	3,200 cps continuous LGC output to reset LR transfer gates.
Range strobe	LGC	Timing pulses to enable LR transfer gates.
V_{xa}, V_{ya}, V_{za} strobe pulses	LGC	Timing pulses to enable LR transfer gates.

Table I-IV. Description of Rendezvous Radar Interface Signals

Signal Name	Source	Description
Antenna shaft angle	RR	Sine and cosine of 1X and 16X shaft angle resolvers.
Antenna shaft command	CDU	Torquing signal from LGC via CDU which changes position of antenna shaft.
Antenna trunnion angle	RR	Sine and cosine of 1X and 16X trunnion angle resolvers.
Antenna trunnion command	CDU	Torquing signal from LGC via CDU which changes position of antenna trunnion.
RR data good	RR	Digital pulses to LGC to indicate that RR is locked on and data is good.
RR in "0" and RR in "1."	RR	Digital pulses to LGC which contain range and range rate data.
Range gate and range rate gate	LGC	Timing pulses to enable RR transfer gates.
Radar gate reset	LGC	Reset pulses for gates.
Counter readout command	LGC	Fifteen pulses from LGC which read out contents of RR output shift register.
Power on and in auto LGC mode	RR	Pulses to indicate RR is on and in auto mode.
RR auto track enable	LGC	Allows RR to lock on return signal.
RR range low scale	RR	Scaling of data has changed to low scaling.

Chapter 2

SYSTEM AND SUBSYSTEM FUNCTIONAL ANALYSIS

2-1 SCOPE

This chapter provides functional descriptions of the PGNCS and its subsystems. This chapter describes how the PGNCS subsystems perform the PGNCS operations.

2-2 PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM.

The PGNCS is functionally divided into three major subsystems: inertial, optical, and computer. The PGNCS performs three basic functions: inertial guidance, navigation, and autopilot stabilization and control. Within these functions the subsystems, or combination of subsystems, with assistance from the astronaut, perform the following operations:

(1) Establish an inertial reference which is used for measurements and computations.

(2) Aligns the inertial reference by optical measurements and, through interface, aligns the inertial reference with the CSM PGNCS.

(3) Calculates the position and velocity of the LEM by inertial navigation.

(4) Accomplishes a LEM and CSM rendezvous by radar tracking, optical navigation, and inertial guidance.

(5) Generate attitude control and thrust commands to maintain the LEM on a satisfactory trajectory.

(6) Control throttling of descent engine during lunar landing.

(7) Display pertinent data related to guidance status.

(8) Controls ascent engine burn time to obtain proper velocity for rendezvous orbit.

To perform its inertial guidance functions, the PGNCS employs an IMU containing accelerometers mounted on a gyro stabilized, gimbal-mounted platform (stable member). The IMU, three channels of the CDU, the pulse torque assembly (PTA), and the PSA form the ISS of the PGNCS.

To perform its navigational functions, the PGNCS employs the AOT, the LR, and the RR. The AOT provides a means of manually taking direct visual sightings and precision angular measurements of preselected celestial targets. During the powered descent and landing phases, the PGNCS receives altitude and velocity data from the LR, which is used to update or check inertially derived data. During the coasting descent, lunar stay, and rendezvous phases, the RR tracks its transponder in the orbiting CSM to provide range, range rate, and antenna angle measurements to the LGC.

The LGC is a digital computer which serves as both the control element and the primary data processing element of the PGNCS. The LGC and the display and keyboard (DSKY) form the computer subsystem of the PGNCS.

Figure 2-1 illustrates the signal flow and interface between the PGNCS subsystems and navigational aids.

2-3 LEM AND PGNCS AXES

Several sets of axes are associated with the LEM and PGNCS. Figure 2-2 illustrates these various orthogonal sets which are defined in the following paragraphs. Positive rotation about each axis is as defined by the right hand rule.

2-3.1 LEM SPACECRAFT AXES. The LEM spacecraft axes provide a reference for all other sets of axes and define the point about which attitude maneuvers are performed. The LEM spacecraft axes, designated X_{LEM}, Y_{LEM}, Z_{LEM}, are referred to as the yaw, pitch, and roll axes respectively. The X_{LEM} axis points through the upper docking hatch and the Z_{LEM} axis points through the forward hatch. The Y_{LEM} axis is perpendicular to the X_{LEM} and the Z_{LEM} axes and can be considered to be pointing out of the astronaut's right shoulder as he faces toward the forward portion of the LEM.

2-3.2 NAVIGATION BASE AXES. The navigation base provides a precise alignment of the IMU to the AOT and the ASA and a means of attaching all three units to the spacecraft. The navigation base is mounted to the LEM structure so that a coordinate reference system is formed by its mounting points. The Y_{NB} axis is defined by the centers of the two upper mounting points and is parallel to the Y_{LEM} axis. The X_{NB} axis is defined by a line through the center of the lower mounting point, perpendicular to the Y_{NB} axis and parallel to the X_{LEM} axis. The Z_{NB} axis is mutually perpendicular to the X_{NB} and Y_{NB} axes and is parallel to the Z_{LEM} axis.

2-3.3 INERTIAL AXES. The inertial axes provide references for measuring changes in velocity and attitude. At zero gimbal angles, the inertial axes are parallel to the navigation base axes.

2-3.3.1 Gimbal Axes. The gimbal axes (outer, middle, and inner) are the axes of the movable gimbals. The axes are defined by the intergimbal assemblies which provide each gimbal with rotational freedom. The attitude of the spacecraft with respect to the stable member is measured by the gimbal resolvers located in the intergimbal assemblies.

2-3.3.2 Stable Member Axes. The stable member axes (X_{SM}, Y_{SM}, Z_{SM}) provide a reference for aligning the inertial components and for defining the angular orientation of the inertial axes during flight.

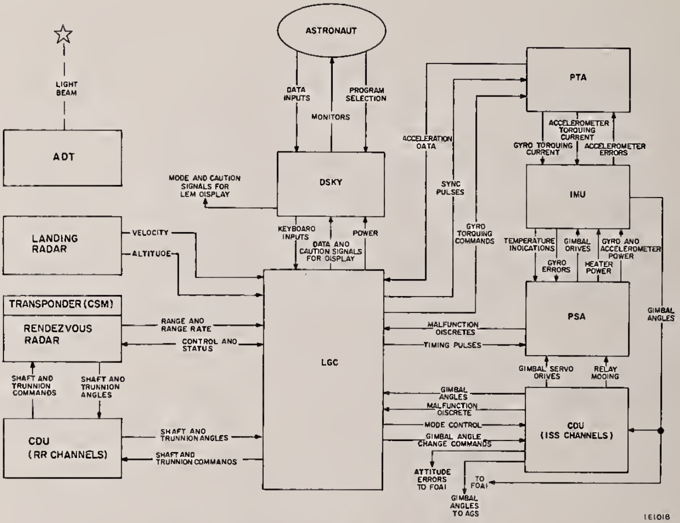
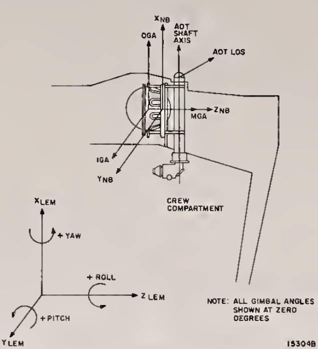


Figure 2-1. PGNCS Internal Interface, Block Diagram



NOTE: ALL GIMBAL ANGLES SHOWN AT ZERO DEGREES

Figure 2-2. LEM and PGNCS Axes

2-3.3.3 Accelerometer Axes. The accelerometer axes (X_a, Y_a, Z_a) are the positive input axes of the accelerometers and are parallel to the stable member axes. Velocity changes are measured along the accelerometer input axes. This velocity data is used to determine spacecraft position and velocity.

2-3.3.4 Gyro Axes. The gyro axes (X_g, Y_g, Z_g) are the positive input axes of the stabilization gyros and are parallel to the stable member axes. If the attitude of the stable member is changed with respect to inertial space, the gyro senses the change about its input axis and provides an error signal to a servo loop which realigns the stable member to its original orientation.

2-4 INERTIAL SUBSYSTEM

The ISS performs three major functions. It measures changes in LEM attitude, assists in generating steering commands, and measures spacecraft velocity due to thrust. To accomplish these functions, the IMU provides an inertial reference consisting of a stable member with a three degree of freedom gimbal system and stabilized by three rate integrating gyros. Each time the inertial subsystem is energized, the stable member must be aligned with respect to a predetermined reference. During flight and prior to launch from the lunar surface, this alignment is accomplished by sighting the optical instrument on celestial objects.

Once the ISS is energized and aligned, any rotational motion of the LEM will be about the stable member, which remains fixed in space. Resolvers mounted on the gimbal axes act as angular sensing devices and measure the attitude of the LEM with respect to the stable member. These angular measurements are displayed by the FDAI and angular changes are sent to the LGC via the CDU.

The desired LEM attitude is calculated in the LGC and compared with the actual gimbal angles. Any difference between the actual and calculated angles results in the generation of attitude error signals by the ISS channels of the CDU which are sent to the FDAI for display.

Vehicle acceleration is sensed by three pendulous accelerometers mounted on the stable member with their input axes orthogonal. The signals from the accelerometers are supplied to the LGC which calculates the total vehicle velocity.

The modes of operation of the inertial subsystem can be initiated automatically by the LGC or by the astronaut selecting computer programs through the DSKY. The status or mode of operation is displayed on the DSKY.

For purposes of explanation and description, the ISS is divided into functional blocks as shown in figure 2-3 and described in the following paragraphs.

2-4.1 STABILIZATION LOOP. The three stabilization loops (figure 2-4) maintain the stable member in a specific spatial orientation so that three mutually perpendicular 16 pulsed integrating pendulum (16 PIP) accelerometers can measure the proper components of LEM acceleration with respect to the coordinate system established by the stable member orientation. An input to the stabilization loops is created by any change in LEM attitude with respect to the spatial orientation of the stable member. Because of gimbal friction and unbalances, motion of the LEM structure relative to the stable member will produce a torque on the stable member which will tend to change its orientation. This change is sensed by the stabilization gyros. When the gyros sense an input, they issue error signals which are amplified, resolved, if necessary, into appropriate components, and applied to the gimbal torque motors. The gimbal torque motors then drive the gimbals until the stable member regains its original spatial orientation.

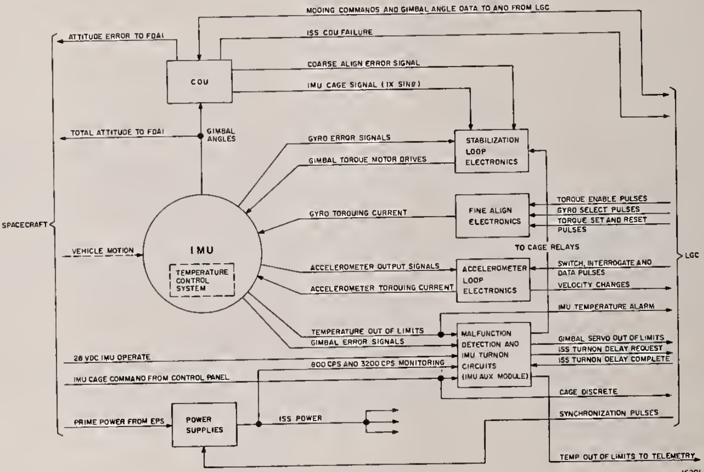

MODING COMMANDS AND GIMBAL ANGLE DATA TO AND FROM LGC
ATTITUDE ERROR TO FDAI
ISS CDU FAILURE
CDU
COARSE ALIGN ERROR SIGNAL
IMU CAGE SIGNAL (1X SIN θ)
TOTAL ATTITUDE TO FDAI
GIMBAL ANGLES
GYRO ERROR SIGNALS
STABILIZATION LOOP ELECTRONICS
GIMBAL TORQUE MOTOR DRIVES
FINE ALIGN ELECTRONICS
TORQUE ENABLE PULSES
GYRO SELECT PULSES
TORQUE SET AND RESET PULSES
GYRO TORQUING CURRENT
SPACECRAFT
TO CAGE RELAYS
VEHICLE MOTION
IMU
TEMPERATURE CONTROL SYSTEM
LGC
ACCELEROMETER OUTPUT SIGNALS
ACCELEROMETER LOOP ELECTRONICS
SWITCH, INTERROGATE AND DATA PULSES
ACCELEROMETER TORQUING CURRENT
VELOCITY CHANGES
IMU TEMPERATURE ALARM
TEMPERATURE OUT OF LIMITS
MALFUNCTION DETECTION AND IMU TURNON CIRCUITS (IMU AUX MODULE)
GIMBAL ERROR SIGNALS
GIMBAL SERVO OUT OF LIMITS
ISS TURNON DELAY REQUEST
28 VDC IMU OPERATE
800 CPS AND 3200 CPS MONITORING
ISS TURNON DELAY COMPLETE
IMU CAGE COMMAND FROM CONTROL PANEL
CAGE DISCRETE
SYNCHRONIZATION PULSES
PRIME POWER FROM EPS
POWER SUPPLIES
ISS POWER
TEMP OUT OF LIMITS TO TELEMETRY
16201

Figure 2-3. ISS, Block Diagram

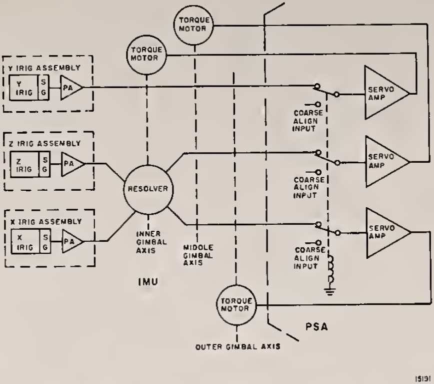


Figure 2-4. Stabilization Loop, Block Diagram

The stabilization loop consists of three pre-aligned Apollo II inertial reference integrating gyro (Apollo II IRIG) assemblies, a gyro error resolver, three gimbal servo amplifiers, three gimbal torque motors, three gimbals, and circuitry associated with these components. The inner gimbal is the stable member upon which the three stabilization gyros are mounted. The gyros are mounted with their input axes oriented in an orthogonal configuration. Movement of any gimbal tends to result in a movement of the stable member and rotation about the input axes of one or more of the stabilization gyros.

The stabilization loop contains three parallel channels. Each channel starts with a stabilization gyro (X, Y, or Z) and terminates in a gimbal torque motor. The torque motor drives the gimbals resulting in a movement of the stable member and a movement of the stabilization gyros. When a movement of the IMU support gimbal attempts to displace the stable member from its erected position, one or more of the stabilization gyros senses the movement and issues error signals. The phase and magnitude of the 3,200 cps gyro error signal represents the direction and amount of rotation experienced by the gyro about its input axis. The error signal is fed from the gyro signal generator ducosyn to the associated IRIG preamplifier, which is a part of the prealigned Apollo II IRIG assembly. Amplification of the error signal is required to achieve a high signal-to-noise ratio through the gimbal slip rings.

The amplified gyro error signals also represent motion of the stable member about its axis since the stable member axes (X_{SM}, Y_{SM}, Z_{SM}) and the gyro axes (X_g, Y_g, Z_g) are parallel to one another.* If the middle and outer gimbal axes remain parallel with the stable member axes, then movement of the outer gimbal (a yaw movement of the LEM) is sensed by only the X gyro and movement of the middle gimbal (roll movement of the LEM) is sensed by only the Z gyro. Movement of the stable member about the inner gimbal axis (Y_{SM}), however, changes the relationship of the X and Z gyro input axes to the outer and middle gimbal axes. As a result, a movement of the middle or the outer gimbal is sensed by both X and Z gyros. The input required by the gimbal servo amplifiers to drive the gimbals and move the stable member back to its original position must be composed of components of both the X and Z gyros. The required gimbal error signals are developed by the gyro error resolver. The gyro error signals, $E(X_g)$ and $E(Z_g)$, are applied to the stator windings of the gyro error resolver. The rotor windings are connected to the inputs of the outer and middle gimbal servo amplifiers. Movement of the stable member about the inner gimbal axis (pitch movement of the LEM) changes the position of the resolver rotor relative to the resolver stator. This change corresponds electromagnetically to the change in the relationship of the stable member axes to the outer and middle gimbal axes. The outputs taken from the rotor are the required middle and outer gimbal error signals (E_{mg} and E_{og}). Since the inner gimbal torque motor axis and the Y axis of the stable member are the same axis, the Y gyro error signal, $E(Y_g)$, is equal to the inner gimbal error signal, (E_{ig}), and is fed directly to the inner gimbal servo amplifier.

The three identical gimbal servo amplifier modules are located in the PSA and contain a phase sensitive demodulator, a filter, and a dc operational power amplifier. The phase sensitive demodulator converts either the 3,200 cps gimbal error or 800 cps coarse align error, zero or pi phase, signals into a representative positive or negative dc signal. The dc signal is filtered and applied to a dc operational amplifier with current feedback. The compensation network in the feedback circuit of the amplifier controls the response characteristics of the entire stabilization loop. The output of the dc amplifier has an operating range between +28 vdc and -28 vdc and drives the respective gimbal torque motor directly in either angular direction.

The gain required for each stabilization loop differs. This difference compensates for the differences in gimbal inertia. The proper gain is selected by the connections to the gimbal servo amplifier module. A single torque motor is mounted on each gimbal at the positive end of the gimbal axis. The torque motors drive the gimbals to complete the stabilization loop.

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* The Z gyro has its positive input axis aligned to the $-Z_{SM}$ axis but this is compensated for by reversing the polarity of the 3,200 cps excitation to the primary winding of the Z gyro signal generator ducosyn which causes the Z gyro error signal to be representative of the direction and amount of motion about the Z_{SM} axis.

The orientation of the stable member can be changed in either the coarse align, fine align, or IMU cage modes. Signals to reposition the gimbals are injected into the gimbal servo amplifiers from the CDU during the coarse align and IMU cage modes and into the stabilization gyros from the fine align electronics during the fine align mode. During the IMU cage mode and the coarse align mode, the reference signal for the demodulator in the gimbal servo amplifier is externally switched from 3, 200 cps to 800 cps.

2-4.2 FINE ALIGN ELECTRONICS. The fine align electronics (figure 2-5) provides torquing current to the stabilization gyros to change the orientation of the IMU gimbals during the fine align mode. The operation of the fine align electronics is controlled by the LGC.

The components of the fine align electronics are common to the three stabilization gyros. The fine align electronics provides torquing signals to the stabilization gyros one at a time on a time shared basis. The fine align electronics consists of a gyro calibration module, a binary current switch module, and a dc differential amplifier and precision voltage reference module, all located in the PTA.

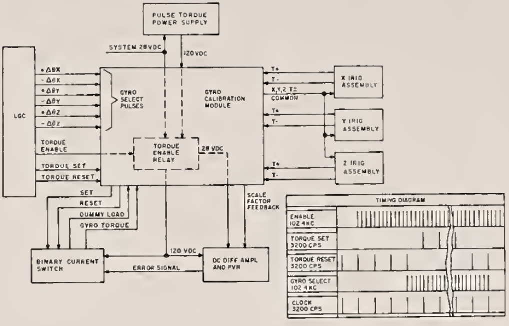

Figure 2-5. Fine Align Electronics - Computer Inputs

The fine align electronics is enabled and controlled by LGC inputs to the gyro calibration module. The LGC inputs consist of torque enable pulses, gyro select pulses, a torque set command, and a torque reset command. The fine align electronics is enabled by the torque enable pulses. The torque enable pulses are a train of pulses three microseconds in width and occurring at 102.4 kpps. The torque enable pulses are applied through a relay driver to energize the torque enable relay in the calibration module. When the torque enable relay is energized, system 28 vdc is applied to the precision voltage reference (PVR) and regulated 120vdc from the pulse torque power supply is applied to the dc differential amplifier and the binary current switch. The torque enable pulse train is received 20 milliseconds prior to any gyro set command.

The gyro to be torqued and the direction it is to be torqued is selected by the LGC by sending gyro select pulses to one of the six $+\Delta\theta$ or $-\Delta\theta$ inputs. (See figure 2-6.) The gyro select pulse consists of a train of pulses three microseconds in width and occurring at 102.4 kpps. The pulse train activates a transistor switch network which controls current through the T+ or T- coils of the torque generator ducosyn in the gyro selected. The gyro select pulse train is received 312.5 microseconds (one LGC clock time at 3,200 pps) prior to any torque set command.

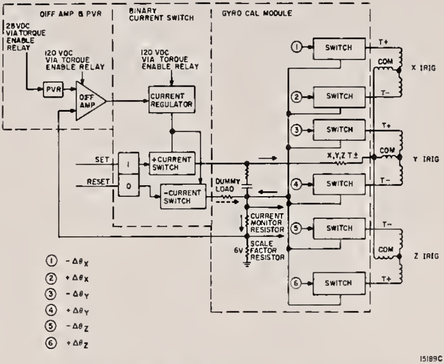

Figure 2-6. Fine Align Electronics - Gyro Selection

The torque set and reset commands are 3,200 pps pulse trains containing pulses that are three microseconds in width. A 3,200 pps pulse train will be present on the torque set line when any gyro is to be torqued. A 3,200 pps pulse train is present on the torque reset line at all other times. This ensures that the binary current switch is in the reset condition prior to receipt of a torque enable command from the LGC. When the gyro has been torqued the proper amount, a torque reset command is issued which causes the torque current to be cut off. The gyro select pulse train will be removed 312.5 microseconds after the torque reset command has been issued. The torque set and torque reset pulses are fed through a 1:2 step-up transformer in the calibration module to the set and reset inputs of the binary current switch.

The torque current from the binary current switch is applied through a tuned resistive-capacitive compensation network in the calibration module to make the torque generator ducosyn windings appear as a pure resistive load to the binary current switch. The torque current to the gyros is via the T±(common) line. Current will flow only through the selected torque generator coils, the current monitor resistor, and the scale factor resistor. The voltage drop developed across the scale factor resistor is used as a feedback to the differential amplifier to regulate the torquing current. The voltage drop across the current monitor resistor is applied to PTA test points for external monitoring of gyro torque current.

When no gyro is being torqued, the binary current switch provides current flow through a dummy load resistor and through the current monitor and scale factor resistors. In this manner, the binary current switch maintains a continuous flow of torque current. The dummy load resistor simulates the impedance of the torque generator coil and a compensation network.

The torque set and torque reset pulses trigger a flip-flop (bi-stable multivibrator) in the binary current switch (figure 2-7). If the flip-flop is in the +set condition, the +set condition will remain until a reset command resets the flip-flop. The outputs of the flip-flop control two transistor switches. If the flip-flop is in the +set condition, the +set output is present at the base of the +torque current switch, causing the switch to turn on. The +torque current switch closes the path from the 120 volt supply through the current regulator to the proper T+ or T- winding of the selected gyro via the calibration module. If the flip-flop is in the -set condition, the -torque current switch will turn on and close the current path through the dummy load resistor.

The binary current switch used in the fine align electronics is identical to the one used in the accelerometer loops. The portion of the binary current switch used only for the accelerometer loops is disabled in the fine align electronics application. In the accelerometer loop application, current to the accelerometer T+ torque generator coil is provided by the +torque current switch and current to the T- torque generator coil is provided by the -torque current switch. Therefore, the +torque and -torque designations of the switches have significance. In the fine align electronics application the switch designations have no significance since current to both the T+ and T- coils of the gyro torque generators is provided by the +torque current switch while the -torque current switch provides only the dummy load current.

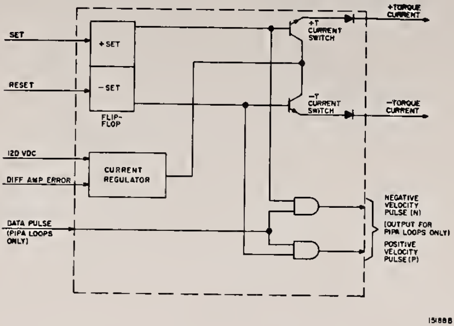

Figure 2-7. Binary Current Switch

The dc differential amplifier and PVR module (figure 2-8) maintains the current through the windings of the torque generator ducosyn at 84 milliamperes. The PVR is supplied with regulated 28 vdc and, through the use of zener diode circuits, develops an accurate 6 vdc for use as a reference voltage. The scale factor resistor in the calibration module also has 6 volts developed across it when 84 milliamperes of current flows through it. A comparison is made by the dc differential amplifier of the PVR 6 volts and the scale factor resistor 6 volts. Any deviation from the nominal 84 milliamperes of torquing current will increase or decrease the voltage developed across the scale factor resistor and cause an output error signal from the dc differential amplifier. This error signal controls the current regulator in the binary current switch. The current regulator, which is in series with the torque generator coils of the selected gyro and the 120 vdc source, will maintain the torquing current at 84 milliamperes.

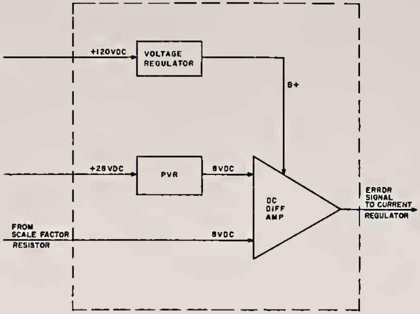

Figure 2-8. DC Differential Amplifier and Precision Voltage Reference

The current flow through the windings of the torque generator ducosyn causes the gyro float to rotate about the gyro's output axis. A $+\Delta\theta$ gyro select command from the LGC will allow torque current to flow through a T- torque generator coil which results in a positive rotation of the gyro float about the output axis. A $-\Delta\theta$ gyro select command produces a negative float rotation.* Float rotation results in an error output from the signal generator ducosyn. The error signal is applied to the stabilization loop to reposition the gimbals and the stable member. The change in gimbal angles is transmitted by the CDU read counters to the LGC.

* The positive input axis of the Z gyro is aligned to the $-Z_{SM}$ axis but this is compensated for by reversing the T+ and T- connections to the Z gyro torque generator ducosyn. A $+\Delta\theta$ Z gyro select command from LGC will cause a negative float rotation but since the polarity of the Z gyro signal generator is also reversed the gyro error signal will appear to represent a positive float rotation. The stabilization loops will then drive the gimbals in the desired direction.

2-4.3 ACCELEROMETER LOOP. The three accelerometer loops measure the acceleration of the stable member along three mutually perpendicular axes and integrate this data to determine velocity. The velocity is used by the LGC to determine the LEM velocity vector. Figure 2-9 is a functional diagram of an accelerometer loop.

The three accelerometer loops contain three prealigned 16 PIP assemblies, three PIP preamplifiers, three ac differential amplifier and interrogator modules, three binary current switches, three calibration modules, three dc differential amplifier and precision voltage reference modules, a pulse torque isolation transformer, and associated electronics.

The three mutually perpendicular PIP's are acceleration sensitive devices. When fixed in its associated accelerometer loop, the PIP becomes an integrating accelerometer. The PIP is basically a pendulum-type device consisting of a cylinder with a pendulous mass unbalance (pendulous float) pivoted with respect to a case. The axis of the pivots defines the PIP output axis. A signal generator is located at the positive end of the output axis to provide electrical output signals indicative of the rotational position of the float. A torque generator located at the other end of the float acts as a transducer to convert electrical signals into mechanical torque about the float shaft. The accelerometer loop using a PIP is mechanized to operate in a binary (two state) mode.

In the binary mode, the PIP pendulum is continually kept in an oscillatory motion. Thus the two states: positive rotation or negative rotation. The rotation is accomplished by continuously routing torquing current through the torque generator plus or minus windings.

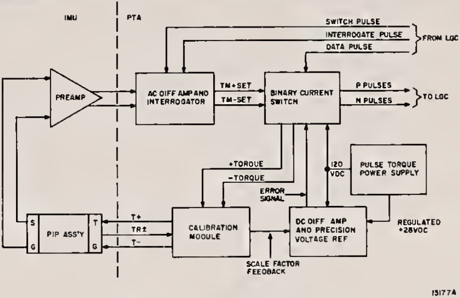

Figure 2-9. Accelerometer Loop

The torque generator has two windings, one to produce torque (rotation) in a positive direction, the other to produce torque (rotation) in a negative direction. Only one winding will have current in it at any one time. The torque winding selection is accomplished by the setting of a flip-flop in the binary current switch (figure 2-7). When the loop is first energized, the interrogator sets the flip-flop to route the torquing current to one of the windings, which will rotate the float to null. As the float passes through null, the phase of the output signal of the signal generator changes, which causes the interrogator to issue pulses to reset the flip-flop in the binary current switch and thus route torquing current to the other torque winding. The float is then torqued in the opposite direction until the signal generator output again changes phase as the float passes through null which reinstates the cycle.

The output of the signal generator, after being amplified by the PIP preamplifier is interrogated 3200 times a second by the interrogate pulse. The binary current switch flip-flop can be reset only when the interrogate pulse is present and the signal generator output is of the proper phase.

The PIP pendulum motion is an oscillatory motion about its null point and can be measured in cycles per second. As is characteristic of every electro-mechanical loop, there exists some natural resonant frequency. The natural frequency is dependent upon float damping, signal and torque generator sensitivities, and other loop characteristics. In the case of the accelerometer loop this natural frequency is approximately 500 cps, and the pendulum oscillates at a frequency close to that. At a torque winding selection rate of 3200 pulses per second, the value of this frequency can be any value equal to $3200 \div x$ where x is any even number.

Using the above ratio, it is possible for the pendulum to have a maximum frequency of 1600 cps (x equals 2). A frequency of 1600 cps means that for every torque selection pulse, the torque current would be routed to the opposite torque generator winding. Solving the equation $f = 3200 \div x$, the frequency closest to 500 is 533-1/3. In this case; the value of x is six. Thus one complete pendulum cycle will occur during six torque selection pulses. Dividing the time for the six pulses into positive and negative rotations, it is seen that the PIP functions in a 3-3 mode (positive rotation for three torque selection pulses, negative rotation for three torque selection pulses).

The physical configuration of the PIP is such that the float, when moding in its 3-3 state and sensing no acceleration, rotates an equal angular distance on both sides of an electrical and mechanical null.

The 2 volt rms, 3200 cps, one phase signal generator excitation voltage is synchronized with the LGC clock. The signal generator has a center tapped secondary winding which provides a double ended output, one side having a zero phase reference with respect to the 3,200 cps excitation and the other side a pi phase reference. The center tap is connected to ground. The output signal is representative of the magnitude and direction of the rotation of the pendulous float about the output axis. The error signal is then routed to the preamplifier mounted on the stable member. The phase of the output signal from the preamplifier is -45° from the reference excitation. The phase shifted zero or pi phase signals from the preamplifier are applied as separate inputs to the ac differential amplifier and further amplified. The two signals are then sent to the interrogator.

The ac differential amplifier and the interrogator are packaged in the same module which is located in the pulse torque assembly (PTA) (figure 2-10). The interrogator analyzes the ac differential amplifier outputs to determine the direction of the 16 PIP float movement and generates appropriate torquing commands. The two amplified signals from the ac differential amplifier go to two summing networks and threshold amplifiers (represented in figure 2-10 by AND gates). Interrogate pulses (IP) are continuously being received by the interrogator from the LGC. An interrogate pulse is a two microsecond pulse occurring at 3,200 pps and timed to occur 135 degrees after the positive going zero crossing of the reference excitation. (See figure 2-11.) With this phasing, the interrogate pulse occurs at the 90 degree peaks of the phase shifted zero or pi phase input signals from the PIP preamplifiers. The interrogate pulse occurs at a positive 90 degree peak of the zero phase signal if the float angle is positive and at a positive 90 degree peak of the pi phase signal if the float angle is negative. The zero and pi phase signals and the interrogate pulses are ANDed by the summing network and threshold amplifier. The gated outputs of the threshold amplifier are applied to a flip-flop as set or reset pulses. If the flip-flop is in the +set condition, a succession of set pulses will maintain the +set condition. The +set condition will remain until the float angle passes through null. At this time, a reset pulse is produced to cause the flip-flop to go to the -set condition.

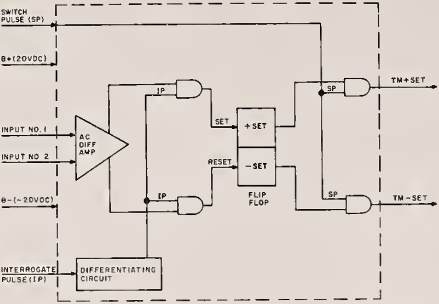

Figure 2-10. AC Differential Amplifier and Interrogator Module

The outputs of the flip-flop are applied to two AND gates which are also driven by switch pulses received from the LGC. The switch pulses are a train of clock driven 3,200 pps pulses three microseconds in width, timed to occur three microseconds after the leading edge of the interrogate pulse. The flip-flop enables only one output gate at any switch pulse time. The outputs of the AND gates are called the TM + set pulse and the TM - set pulse.

The binary current switch (figure 2-7) utilizes the TM + set and TM - set outputs of the interrogator to generate 16 PIP torquing current. The TM + set and the TM - set pulses furnish the input to a flip-flop. If the flip-flop is in the +set condition, a succession of TM + set pulses will maintain the +set condition. The +set condition will persist until the float angle passes through null. The phase change will cause the flip-flop of the ac differential amplifier and interrogator module to reset to the -set condition. At this time a TM - set pulse is developed and causes the binary current switch flip-flop to go to the -set condition. The outputs of the flip-flop control two transistor current switches. If the flip-flop is in the +set condition, the +set output will be at the base of the +torque current switch and will turn it on. The +torque current switch closes the path from the current regulated 120 vdc supply through the PIPA calibration module to the 16 PIP T+ torque generator coils. If the flip-flop is in the -set condition, the -torque current switch will be turned on, closing the path through the T- torque generator coils.

An acceleration along the PIP input axis causes the pendulous mass to produce a torque which tends to rotate the float about the output axis. The torque produced by the acceleration is proportional to the magnitude of the acceleration. The acceleration produced torque aids and opposes the torque generator forces causing changes in the time required for the float to be torqued back through null. A change in velocity (ΔV) is the product of acceleration and incremental time (Δt), the torque is actually proportional to an incremental change in velocity (ΔV).

$$T_{ACCEL} = K_1 a \Delta t = K_1 \Delta V$$

The float is already in motion due to loop torquing, therefore additional torque is required to overcome the acceleration torque and to keep the pendulum in its oscillatory motion. The additional torque is obtained by supplying torquing current for additional time through one of the torque windings. The current at any one time is a constant, therefore the current must be present for a longer period of time. Thus to determine the amount of acceleration sensed by the PIP, it is necessary only to measure the length of time torquing current is applied to each torque winding.

$$ACCEL_{IND} = K_2 \Sigma \left[(T+) - (T-)\right] \Delta t$$

From the above identities, it is seen that torquing time (Δt) is proportional to the change in velocity (ΔV).

$$K_1 \Delta V = K_2 \Sigma \left[(T+) - (T-) \right] \Delta t$$

$$\Delta V = \frac{K_2}{K_1} \Sigma \left[(T+) - (T-) \right] \Delta t$$

The time (Δt), representative of the ΔV, is sent to the LGC in the form of P and N pulses (figure 2-9).

In addition to selecting the proper torque generator winding, the outputs of the binary current switch flip-flop also go to two AND gates where they are ANDed with the 3,200 cps data pulses from the LGC. The data pulse is three microseconds in width and is timed to occur two microseconds after the leading edge of the switch pulse. (See figure 2-11.) The data pulse and switch pulse are both 3,200 cps, therefore the LGC receives either a P pulse or an N pulse once every 1 ÷ 3200 second. When the PIP is sensing no acceleration, the pendulum is oscillating at a frequency of 533-1/3 cps; and the LGC is receiving three P pulses and three N pulses once every cycle or once every 1 ÷ 533-1/3 seconds. The LGC contains a forward-backward counter which receives the velocity pulses and detects any actual gain in velocity.

The counter counts forward on the three P pulses and then backward on the three N pulses. The counter continues this operation and generates no ΔV pulses. With an acceleration input to the PIP, however, the loop no longer operates at the 3-3 ratio and the counter exceeds its capacity and reads out the plus or minus ΔV pulses which are then stored and used by the LGC. The additional pulses above the 3-3 ratio are representative of the additional torque supplied by the torque generator to compensate for the acceleration felt by the LEM. Each pulse indicates a known value of ΔV due to the loop scale factor.

The PIPA calibration module (figure 2-12) compensates for the inductive load of the 16 PIP torque generator ducosyns and regulates the balance of the plus and minus torques. The calibration module consists of two load compensation networks for the torque generator coils of the 16 PIP. The load compensation networks tune the torque generator coils to make them appear as a pure resistive load to the binary current switch. A variable balance potentiometer regulates the amount of torque developed by the torque generator coils. Adjustment of this potentiometer precisely regulates and balances the amount of torque developed by the T+ and T- torque generator coils. This balancing insures that for a given torquing current an equal amount of torque will be developed in either direction.

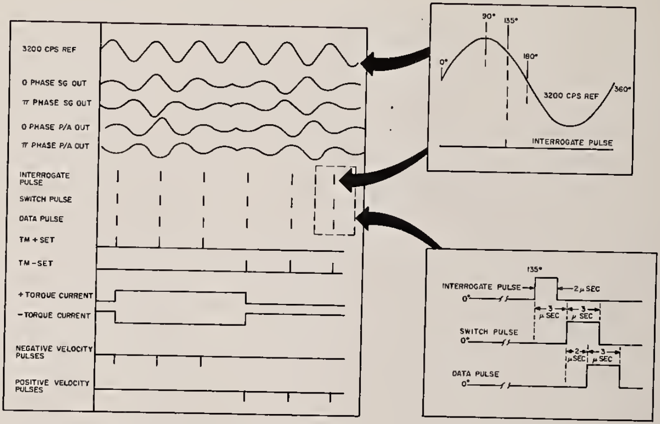

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Figure 2-11. Accelerometer Timing

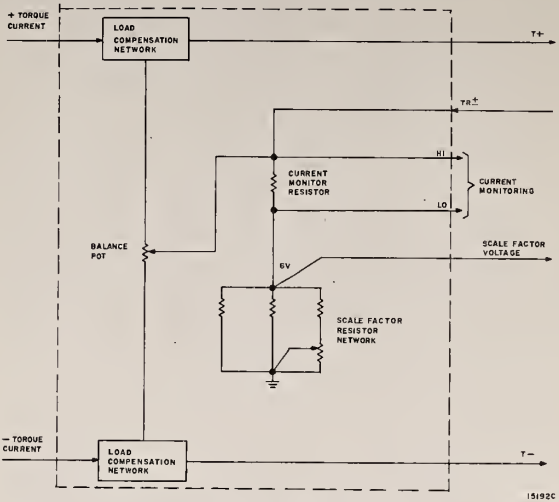


Figure 2-12. PIPA Calibration Module

The calibration module also includes a current monitor resistor and an adjustable scale factor resistor network in series with the torque generator coils. A nominal six volts is developed across the scale factor resistor network due to the torquing current and is applied as an input to the dc differential amplifier and precision voltage reference module. The voltage drop across the current monitor resistor is used for external monitoring purposes.

The dc differential amplifier and PVR are identical to the ones used in the fine align electronics. (See figure 2-8.) The dc differential amplifier and PVR module maintain the current through the ducosyn torque generator coils at a set value which produces the proper scale factor (approximately 43 milliamperes). The PVR is supplied with regulated 28 vdc and, through the use of precision circuits, develops a stable 6 volts (nominal) for use as a reference voltage. The scale factor resistor in the calibration module also develops 6 volts when the set value of current flows through it. A comparison is made by the dc differential amplifier of the PVR 6 volts and the scale factor 6 volts. Any deviation of the torquing current from the set value increases or decreases the scale factor resistor voltage and results in an output error signal from the do differential amplifier. This error signal controls the current regulator in the binary current switch. The current regulator, which is in series with the 120 vdc source and the ducosyn torque generator coils, maintains the torque current at the set value.

2-4.4 IMU TEMPERATURE CONTROL SYSTEM. The IMU temperature control system (figures 2-13 and 2-13A) maintains the temperature of the stabilization gyros and accelerometers within the required temperature limits during both standby and operating modes of the IMU. The system supplies and removes heat to maintain the IMU heat balance. Heat is removed by convection, conduction, and radiation. The natural convection used during IMU standby mode changes to blower controlled, forced convection during IMU operating modes. The IMU internal pressure is maintained between 3.5 and 15 psia to enable the required forced convection. To aid in removing heat, a water-glycol solution at approximately 45 degrees Fahrenheit from the spacecraft coolant system passes through the coolant passages in the IMU case.

2-4.4.1 Temperature Control Circuit. The temperature control circuit maintains the gyro and accelerometer temperature. The temperature control circuit consists of a temperature control thermostat and heater assembly, a temperature control module, three IRIG end mount heaters. three IRIG tapered mount heaters, two stable member heaters, and three accelerometer heaters. The thermostat and heater assembly is located on the stable member and contains a mercury-thallium thermostat. a bias heater, and an anticipatory heater. Except for the bias heater, all heaters (a total of 12) are connected in parallel and are energized by 28 vdc through an switching action of transistor Q2, which completes the dc return path. The thermostat acts as a control sensing element and senses the temperature of the stable member.

When the thermostat temperature falls below 130 (±0.2) degrees Fahrenheit, the thermostat opens and transistor Q1 conducts and drives transistor Q2 to conduction. When transistor Q2 conducts, current will flow through the twelve heaters. Because of the large mass of the stable member, its temperature will increase at a relatively slow rate as compared to the gyros, which have a heater in each end mount. The anticipatory heater improves the response of the thermostat to insure that the magnitude of the temperature cycling of the gyros and the accelerometers is as small as possible. When the thermostat temperature rises above 130 (±0.22) degrees Fahrenheit, the thermostat closes and the base of transistor Q1 is shorted to ground, cutting off transistors Q1 and Q2 and deenergizing the heaters. The temperature control circuit will maintain the average of the gyro temperatures at 135 degrees Fahrenheit and the average of the accelerometer temperatures at 130 degrees Fahrenheit with the specified coolant temperature. The temperature difference between the gyros and the accelerometers is adjusted by properly proportioning the amount of power in each heater.

During IMU operation, power is applied to the fixed accelerometer heaters to compensate for the additional heat supplied to the gyros by the gyro wheel motor heat dissipation. Power is also applied to a bias heater on the control thermostat. The bias heater supplies a fixed amount of heat to the control thermostat to maintain the proper absolute temperature level of the gyros and accelerometers. The amount of bias heat is controlled by the selection of resistor R5. The power for the fixed accelerometer heaters and the thermostat bias heater are the -90 degree and -180 degree outputs, respectively, from the 28 vac power supplies which are also used for gyro wheel power.

The 28 vdc heater power is applied to the heaters through the contacts of a safety thermostat which will provide protection against an extreme overheat condition in case a malfunction occurs in the temperature control circuit. The safety thermostat contacts open at 139.5 (±3.0) degrees Fahrenheit and close at 137 (±3) degrees Fahrenheit.

2-4.4.2 Blower Control Circuit for PGNCS 601 and 602. The blowers maintain IMU heat balance by removing heat. The blowers operate continuously during IMU operate modes. The blower control circuit shown on figure 2-13 is inoperative because the contacts of blower control relay K1 are bypassed.

The blowers are supplied from the -90 and -180 degree outputs of the 28 volt, 800 cps, power supplies which also provide gyro wheel motor power. Fused phase shift networks are associated with each blower so that excitation and control current can be supplied from the same source.

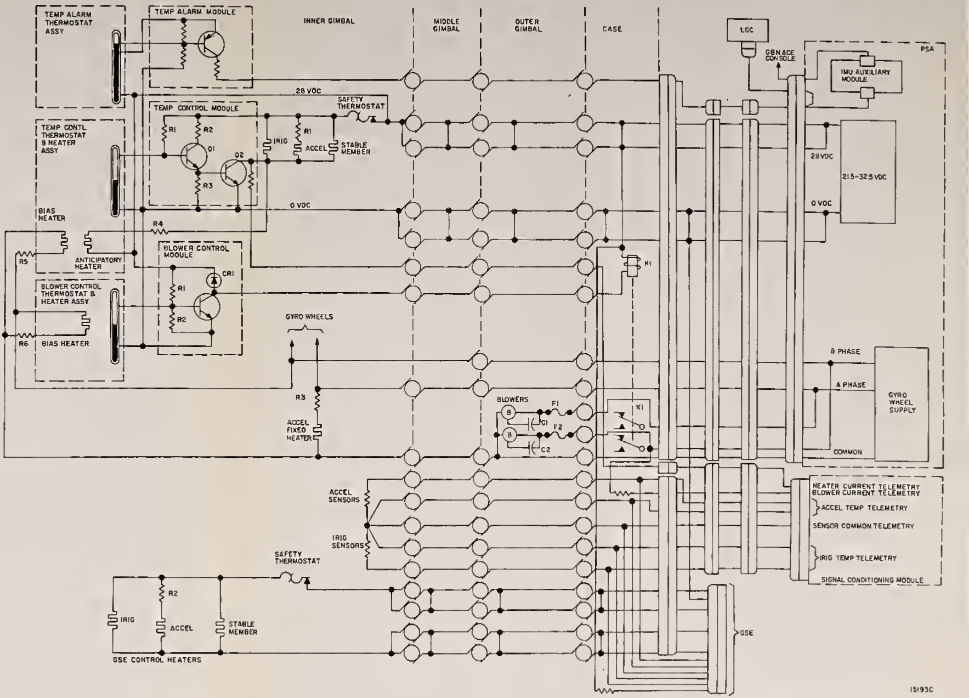


Figure 2-13. IMU Temperature Control System PGNCS 601 and 602

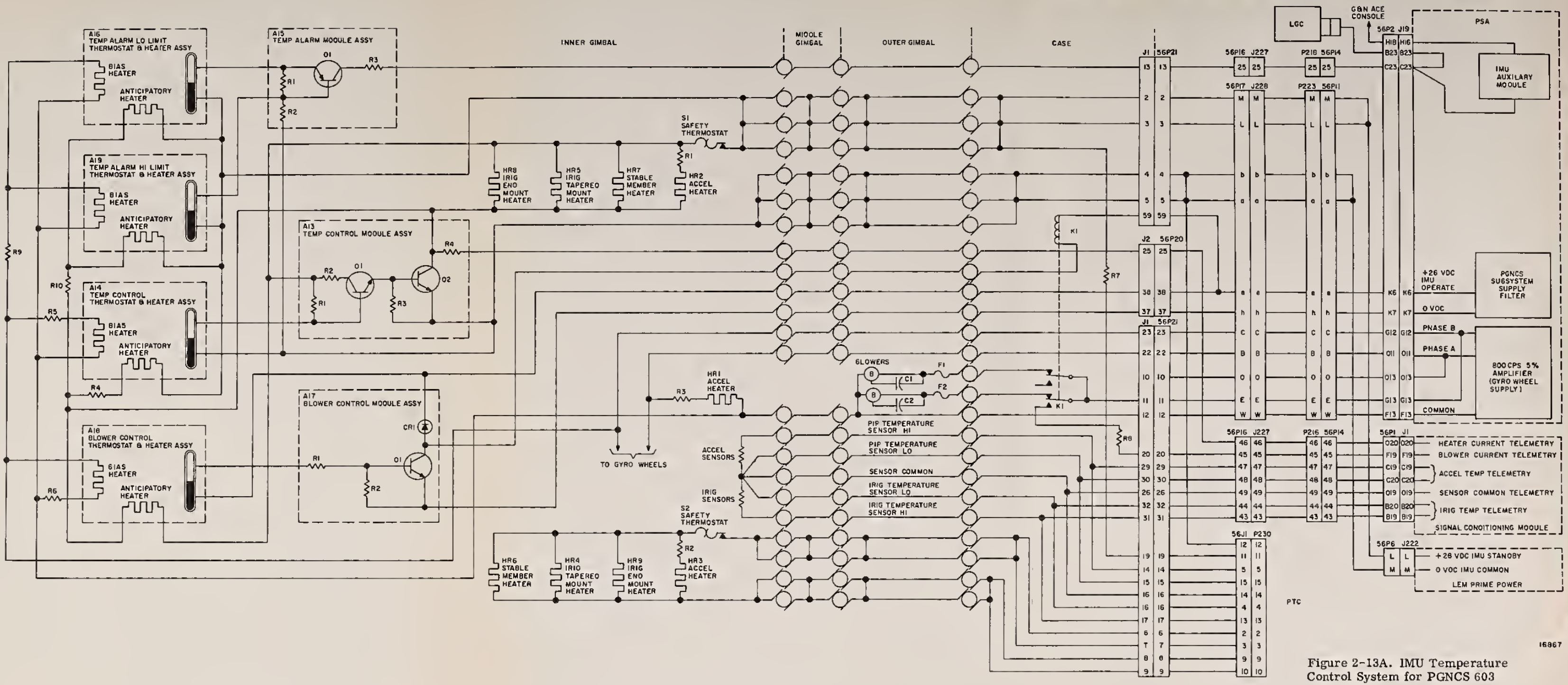


Figure 2-13A. IMU Temperature Control System for PGNCS 603

2-4.4.2A Blower Control Circuit for PGNCS 603. The blower control circuit (figure 2-13A) maintains IMU heat balance by removing heat. The blower control circuit consists of a blower control thermostat and heater assembly, a blower control module assembly, two axial blowers, and a relay. The contacts of the thermostat contained in the blower control thermostat and heater assembly close at 139 (±0.2) degrees Fahrenheit and remain closed at higher temperatures. Resistor R6 is provided to limit the current through the bias heater in the blower control thermostat and heater assembly. The amount of heat supplied by the bias heater is a constant. If the duty cycle of the temperature control circuit exceeds 50 percent, enough additional heat will be provided by the anticipatory heater to increase the temperature of the blower control thermostat and heater assembly to 139 degrees Fahrenheit. When the thermostat contacts close, transistor Q1 conducts and relay K1 is energized to remove the power from the blowers. The normal duty cycle of the temperature control circuit, with the IMU in a 75 degree Fahrenheit ambient temperature, is approximatcly 15 to 20 percent. Under this condition the blowers will operate continuously. Only a very low ambient temperature will cause a blower off condition.

Power to the blowers is supplied from the -90 degree output of the 28 volt, 800 cps, 5 percent power supply which also provides gyro wheel motor power. Fused phase shift networks are associated with each blower so that excitation and control current can be supplied from the same source.

2-4.4.3 Temperature Alarm Circuit for PGNCS 601 and 602. The temperature alarm circuit (figure 2-13) monitors the temperature control system. The temperature alarm circuit consists of a temperature alarm thermostat and a temperature control module. If a high or low temperature is sensed by the temperature alarm thermostat located on the stable member, a discrete is sent to the LGC and the IMU auxiliary module. When the temperature is within the normal range of 126.3 to 134.3 degrees Fahrenheit, 28 vdc is applied through the thermostat to the emitter of transistor Q1 causing the transistor to conduct. Transistor Q1 conducts through a grounding system in the LGC.

When the temperature falls below 126.3 degrees Fahrenheit, 28 vdc will be removed from transistor Q1, causing it to stop conducting and thus signaling the LGC of an alarm condition. When the temperature rises above 134.3 degrees Fahrenheit, 28 vdc will be applied directly to the base of the transistor as well as to the emitter. With 28 volts applied to both emitter and base, the base-emitter junction is no longer forward biased and the transistor stops conducting which signals the LGC of an alarm condition. There is no differentiation between a high or low temperature alarm. When the LGC senses a temperature alarm, it causes the IMU TEMP lamp and the PGNCS lamp to light. When the IMU auxiliary module receives a temperature alarm, it sends the information to telemetry.

2-4.4.3A Temperature Alarm Circuit for PGNCS 603. The temperature alarm circuit which monitors the temperature control system, consists of a temperature alarm high limit thermostat and heater assembly, a temperature alarm low limit thermostat and heater assembly, and a temperature alarm module assembly. If a high or low temperature is sensed by the thermostats located on the stable member a discrete is sent to the LGC and to the IMU auxiliary module. When the temperature is within the normal range, the low limit thermostat contacts are closed and the high limit thermostat contacts are open. Transistor Q1 is then properly biased for conduction through a grounding system in the LGC.

At temperatures below 126.0 (±0.2) degrees Fahrenheit both the low limit thermostat contacts and the high limit thermostat contacts are open. At temperatures above 134.0 (±0.2) degrees Fahrenheit both the low limit thermostat contacts and the high limit thermostat contacts are closed. In either case, transistor Q1 is not able to conduct. Non-conduction of transistor Q1 signals the LGC of an alarm condition. There is no differentiation between a high or low temperature alarm. When the LGC senses a temperature alarm, it causes the TEMP and PGNCS lamps to light. When the IMU auxiliary module receives a temperature alarm, it sends the information to telemetry.

2-4.4.4 External Temperature Control. External temperature control of the IMU is provided by GSE control heater circuits in the IMU which are controlled externally to the airborne equipment by the portable temperature controller (PTC) or the temperature monitor control panel of the optics-inertial analyzer (OIA). The GSE control heater circuitry consists of a safety thermostat, six gyro heaters, two stable member heaters, three accelerometer heaters, temperature indicating sensors, and an IMU standby power sensor which disables the GSE when airborne power is on. The temperature indicating sensors act as the control sensing element of the external control and indicating circuitry. The heaters are connected in parallel. The six gyro temperature indicating sensors (two in each gyro) are connected in series to sense the average temperature of the gyros. The three accelerometer temperature indicating sensors (one in each accelerometer) are connected in series to sense the average temperature of the accelerometers. All of the GSE control heater circuitry is electrically independent of the airborne temperature control system and will not be used at the same time that the IMU temperature is being controlled by the airborne temperature control system. The GSE control heater circuitry cannot be used as a backup temperature control system during flight.

2-4.5 ISS MODES OF OPERATION. The ISS has four major modes of operation: IMU turn on, CDU zero, coarse align, and inertial reference. Submodes which will also be discussed are fine align, IMU cage, attitude error indication and display inertial data. An additional mode is the master reset condition which is available during laboratory testing only. All ISS moding is initiated and controlled by computer discretes to the CDU. (See figure 2-14.) To select an ISS mode of operation, the LGC can send a single discrete, a combination of discretes, or no discretes. The display inertial data function utilizes the RR channels of the CDU; therefore, a description of the discretes to the RR channels of the CDU will also be presented.

2-4.5.1 CDU Discretes. All LGC discretes issued to the CDU to initiate and control the various ISS modes or functions are 0.0 (±2) vdc, LGC ground, applied through a 2,000 ohm source impedance to the CDU mode module.

2-4.5.1.1 ISS CDU Zero. The ISS CDU zero discrete zeros or clears all three ISS CDU read counters simultaneously. It also inhibits the transmission of incrementing pulses to the read counters for the period of time the discrete is present. The CDU discrete will be present (minimum duration is approximately 400 milliseconds) for as long as the read counters are to be held at zero. The IMU is not disturbed by the CDU zero discrete.

2-4.5.1.2 ISS Enable Error Counter. The ISS enable error counter discrete enables all three ISS error counters simultaneously which allows them to accept incrementing pulses from the LGC. The error counters are normally cleared and inhibited. The ISS enable error counter discrete is used in conjunction with the coarse align enable discrete during the coarse align mode. The ISS enable error counter discrete is used alone when display of attitude error signals on the FDAI is required only.

2-4.5.1.3 Coarse Align Enable. The coarse align enable discrete enables a relay driver which energizes the coarse align and demodulator reference relays located in the PSA. This connects the coarse align error signal to the gimbal servo amplifiers and changes the reference voltage for the demodulator in the gimbal servo amplifiers from 3,200 cps to 800 cps. The discrete also enables the digital feedback pulses from the read counter to the error counter. The presence of the coarse align enable discrete and the absence of the enable error counter discrete also inhibits the incrementing pulses to the read counter.

2-4.5.1.4 D/A Enable. The D/A enable discrete enables both RR CDU error counters simultaneously. The error counters are normally cleared and inhibited. The LGC normally provides positioning signals to the RR through the RR channels of the CDU. The D/A enable discrete, however, is also used in conjunction with the display inertial data discrete to allow the LGC to feed inertially derived velocity data through the RR channels of the CDU to meter displays.

2-4.5.1.5 Display Inertial Data. The display inertial data discrete energizes relays which switch the dc output from the digital to analog (D/A) converter in the RR channels of the CDU to the LEM velocity meters.

2-4.5.1.6 RR CDU Zero. The RR CDU zero discrete clears both RR read counters simultaneously and inhibits the transmission of incrementing pulses to the read counters. This discrete is not used for any ISS flight modes or functions but can be used for CDU test functions.

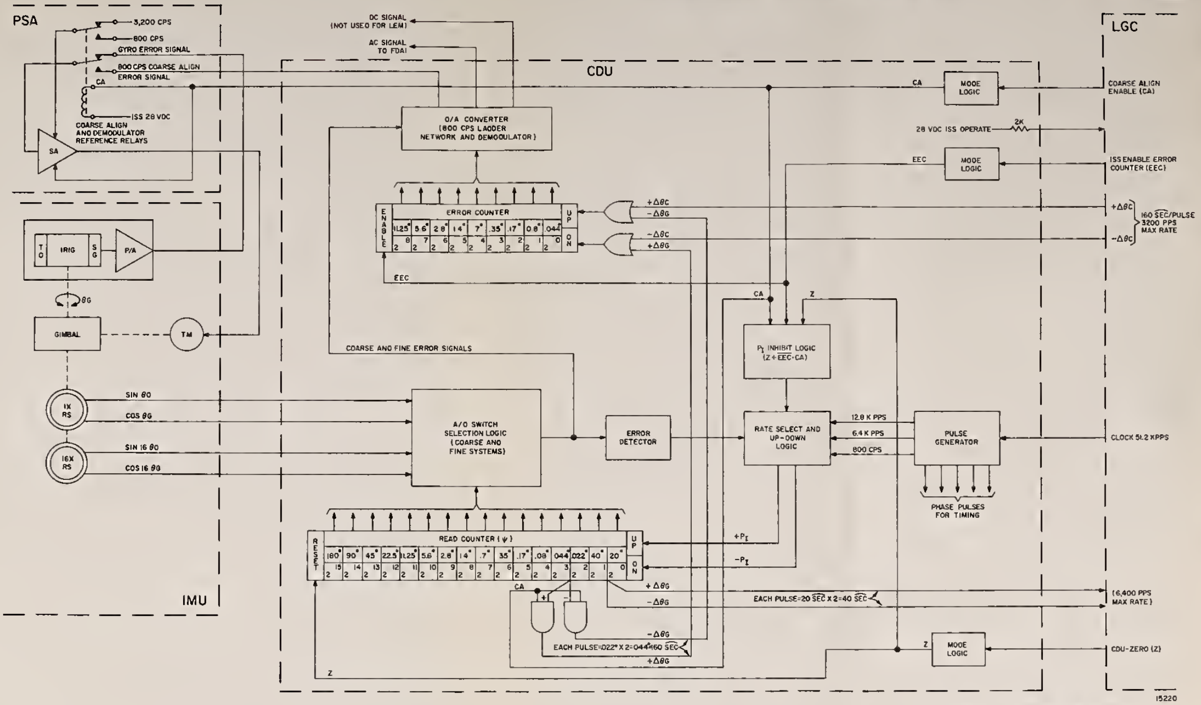


Figure 2-14. ISS-CDU Moding

2-4.5.2 IMU Turn On Mode. The purpose of the IMU turn on mode is to drive the gimbals to their zero position and hold them there. (See figure 2-15.) The IMU turn on mode is initiated upon closure of the ISS OPERATE circuit breaker and allows for a 90 second gyro run up period. The ISS OPERATE circuit breaker routes 28 vdc IMU operate power through the deenergized contacts of the ISS turn on control relay, located in the IMU auxiliary assembly module, to the cage relays. The 28 vdc IMU operate power is also routed through the same deenergized contacts to the LGC as a continuous turn on delay request discrete. The cage relays energize and, in turn, cause the coarse align relays to be energized. The cage relays route the 1X gimbal resolver sine winding outputs through the contacts of the coarse align relays to the respective gimbal servo amplifiers. The gimbal servo amplifiers drive the gimbals until the resolver signals are nulled. The operation of the caging loops is discussed further in the IMU cage mode description.

Upon receipt of the ISS turn on delay request discrete, the LGC sends the ISS CDU zero discrete and the coarse align enable discrete to the CDU for a minimum period of 90 seconds. The CDU zero discrete clears the read counters and inhibits the incrementing pulses to the read counters. The coarse align enable discrete provides a redundant means of energizing the coarse align relays.

A second set of deenergized contacts on the ISS turn on control relay routes a ground to the time delay circuit of the pulse torque power supply which inhibits the operation of the power supply and thus prevents accelerometer pulse torquing during the 90 second turn on period. This allows time for the accelerometer floats to become centered and the gyro wheels to run up prior to torquing.

After the 90 second delay has been completed, the LGC sends the ISS turn on delay complete discrete. The ISS turn on delay complete discrete acts through a relay driver to energize and latch in the ISS turn on control relay. Energizing the ISS turn on control relay deenergizes the cage relay, removes the ISS turn on delay request discrete, and removes the inhibit from the pulse torque power supply. The computer program can then place the ISS in the inertial reference mode by removing both the CDU zero and the coarse align enable discretes, or it can initiate the coarse align mode by removing only the CDU zero discrete and sending the ISS enable error counter discrete. The IMU turn on circuit will be reset whenever 28 vdc IMU operate power is turned off.

2-4.5.3 IMU Cage Mode. The IMU cage mode is an emergency backup mode which allows the astronaut to recover a tumbling IMU by setting the gimbals to zero. (See figure 2-15.) During this mode, the 1X gimbal resolver sine winding outputs are fed through the CDU to the gimbal servo amplifiers to drive the gimbals until the resolver signals are nulled.

The IMU cage mode is initiated when the astronaut presses the IMU CAGE switch. The switch is held until the gimbals settle at the zero position (five seconds maximum). The gimbal position may be observed on the FDAI. The IMU CAGE switch routes a 28 vdc discrete signal to the LGC and to the cage relays located in the PSA. (See figure 2-15.) The cage discrete energizes the cage relays, which in turn, cause the coarse align relays, the demodulator reference relay, and a relay in the gimbal servo amplifiers to energize. The relay in the gimbal servo amplifiers switches in additional capacitance into the RC compensation networks to tune them for 800 cps operation. The demodulator reference relay changes the gimbal servo amplifier demodulator reference signal from 3,200 cps to 800 cps. The cage relays switch the 1X gimbal resolver sine winding outputs through the energized contacts of the coarse align relays into the corresponding gimbal servo amplifier inputs. The gimbal servo amplifiers drive the gimbals until the resolver signals are nulled.

Upon receipt of the IMU cage discrete, the LGC will discontinue sending the error counter enable discrete, the coarse align enable, the display inertial data discrete, and the incrementing pulses to the CDU. The LGC will also discontinue sending torquing commands, if any are in process, to the fine align electronics.

After the IMU CAGE switch is released, the LGC will allow the read counters to settle and will then place the PGNCS in an attitude control mode. During the time the IMU cage discrete is present and while the read counters are settling, the NO ATT lamp on the DSKY is lighted.

The cage mode will also be entered automatically if the IMU is turned on when the LGC is off or in standby mode. During the normal turn on sequence, the closure of the ISS OPERATE circuit breaker will route 28 vdc through the deenergized contacts of the ISS turn on control relay to the cage relays. The cage relays energize and cage the gimbals. After the 90 second turn on time delay has been completed, the LGC will send the ISS turn on delay complete discrete which will energize the ISS turn on control relay which, in turn, deenergizes the cage relays. If, however, the LGC is off or in standby when the IMU is turned on, the ISS turn on control relay will remain deenergized and the ISS will remain in the IMU cage mode.

If the IMU cage mode is entered as a result of an IMU turn on with the LGC off or in standby, the ISS can be placed in the inertial reference mode by allowing 90 seconds for gyro runup then pressing the IMU CAGE switch. The IMU CAGE switch will energize and latch in the ISS turn on control relay which removes the 28 vdc which had been energizing the cage relays. With the ISS turn on control relay latched, the cage relays will deenergize and remain deenergized when the IMU CAGE switch is released. Deenergizing the cage relays causes the coarse align relays to be deenergized which connects the gyro error signals to the respective gimbal servo amplifiers. The stabilization loops will maintain the stable member inertially referenced to the orientation established by the caging loops.

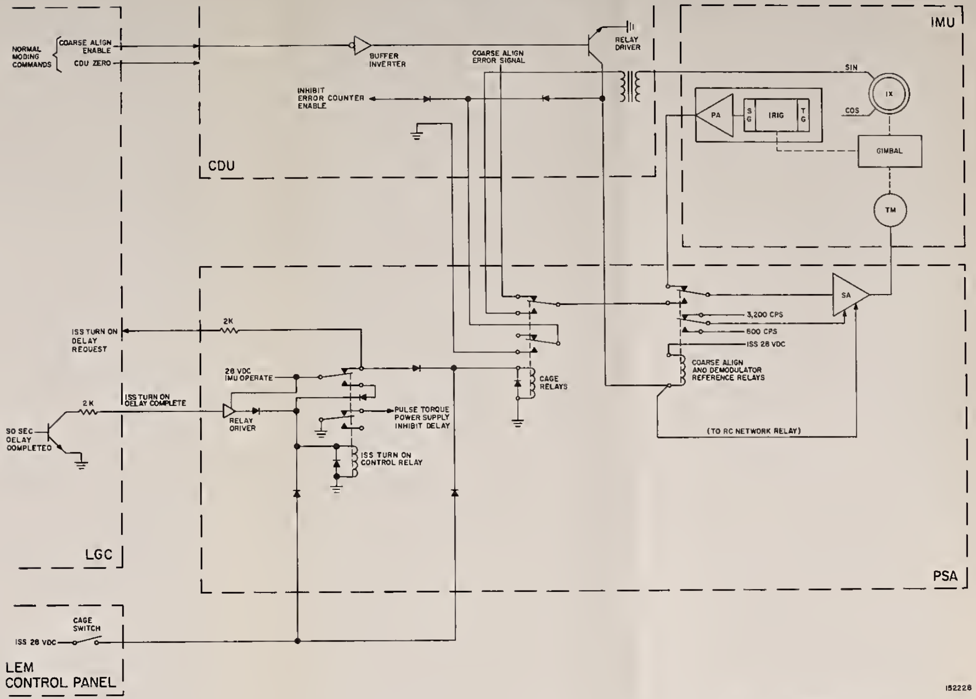


Figure 2-15. IMU Cage Mode

2-4.5.4 ISS CDU Zero. The purpose of the ISS CDU zero mode is to clear and inhibit the three ISS CDU read counters. (See figure 2-14.) The mode is initiated by the LGC sending the ISS CDU zero discrete. The presence of the discrete is maintained for as long as the read counters are to be held at zero.

2-4.5.5 Coarse Align Mode. The purpose of the coarse align mode is to change the orientation of the gimbals by LGC command. The change in gimbal orientation is accomplished by feeding the CDU error counter computer pulses equal to the required change in gimbal angles. The mode is initiated when the LGC sends the coarse align discrete and, after a short delay, the ISS error counter enable discrete to the three ISS channels of the CDU. The LGC, knowing the actual gimbal angle registered in the read counter, calculates the desired amount of change in gimbal angle required to reposition the gimbal to the desired angle and converts this change into a number of $+\Delta\theta_c$ pulses to be sent to the error counter. The $+\Delta\theta_c$ pulses are sent to the error counter at a rate of 3,200 pps in bursts. Each $\Delta\theta_c$ pulse is equal to a change in gimbal angle of approximately 158 arc seconds. The error counter, having been enabled, accepts the pulses and counts up or down, as necessary, until all the pulses have been registered.

The digital information in the error counter is converted into an 800 cps, amplitude modulated, analog error signal by the ladder decoder in the D/A converter module. The ladder decoder signal is summed with a feedback signal and applied through a mixing amplifier located in the D/A converter module to the gimbal servo amplifiers to drive the gimbals to the desired angles. The function of the feedback signal and the mixing amplifier will be discussed later. The output of the mixing amplifier, referred to as the coarse align error signal, is applied to the gimbal servo amplifiers through the contacts of the coarse align relays located in the PSA. The coarse align relays, which are energized by the coarse align enable discrete acting through a relay driver, switch the input of gimbal servo amplifiers from the gyro preamplifiers to the coarse align error signal output of the ISS D/A converters. The demodulator reference relay is also energized by the coarse align enable discrete and switches the reference frequency of the demodulator in the gimbal servo amplifiers from 3,200 cps to 800 cps. The coarse align enable discrete also energizes a relay in the gimbal servo amplifiers which switches in additional capacitance into the amplifier's compensation networks to tune them for 800 cps operation.

As the gimbals are driven, pulses, representing the change in actual gimbal angle, are generated by the read counter and applied to the error counter. These pulses are also equal to approximately 158 arc seconds and act to decrease the $\Delta\theta_c$ pulses registered in the error counter. The error counter output to the ladder decoder, therefore, represents the difference between the desired amount of change in gimbal angle and the amount of change actually accomplished. When the error counter reaches a null and the gimbals stop moving, the actual gimbal angle has changed by an amount equal to the total value of the $+\Delta\theta_c$ pulses sent by the LGC to the error counter. The LGC checks the content of the read counters 2.1 seconds after sending the last $\Delta\theta_c$ pulse to the error counters. If the gimbal angles are not within two degrees of the desired angles, the LGC issues an alarm.

The rate at which the gimbals are driven is limited to prevent damage to the gyros and to assure that the read counter can track the gimbal angle accurately. The rate of gimbal movement is limited by feeding back the CDU fine error signal [sin 16 $(\theta - \psi)$] to the input of the mixing amplifier located in the D/A converter module. The CDU fine error signal is out of phase with the output of the ladder decoder and has an amplitude proportional to the difference between the actual gimbal angle (θ) and the angle in the read counter (ψ). The fine error signal is applied through a voltage limiting circuit to the summing junction of the mixing amplifier where it is summed with the 800 cps ladder decoder output signal. The D/A converter ladder decoder output is applied to the mixing amplifier through a scaling amplifier and a voltage limiting diode network. The scaling amplifier controls the signal gain to produce a scale factor of 0.3 volt rms per degree. The output of the mixing amplifier will be at a null when the D/A converter ladder decoder output, after limiting, is equal to the fine error feedback signal. The fine error signal will be a constant value only when the gimbal and the CDU are going at the same rate and with the gimbal angle leading the CDU angle. Since the CDU is limited to counting at one of two speeds, the gimbals will be limited to a rate equal to one of these two speeds. During the coarse align mode, the CDU is limited to a high counting speed of 6.4 kpps and a low counting speed of 800 cps. At all other times, the high counting speed is 12.8 kpps.

If the gimbals are moving at a faster rate than the rate at which the CDU is counting, the fine error signal will increase, causing a retarding torque to be developed by the gimbal servo amplifier. If the gimbals are moving at a rate slower than the rate at which the CDU is counting, the fine error signal will decrease, causing the gimbal servo amplifier to apply an accelerating torque to the gimbals. By adjusting the gain of the fine error signal into the mixing amplifier, the gimbal drive rate is limited to either 35.5 degrees per second (6.4 kpps CDU counting rate) or 4.5 degrees per second (800 cps CDU counting rate).

2-4.5.6 Inertial Reference Mode. The inertial reference mode provides a coordinate reference system on which attitude and velocity measurements and calculations may be based. During the inertial reference mode, the stable member is held fixed with respect to an inertial reference by the stabilization loops. The ISS CDU read counters provide the LGC with changes in gimbal angles with respect to the stable member. The ISS is in the inertial reference mode during any operating period in which there is an absence of moding commands. During the inertial reference mode, the fine align electronics is inhibited and the ISS CDU error counters are cleared and inhibited.

2-4.5.7 Fine Align Mode. The purpose of the fine align mode is to reposition the stable member to a fine alignment by torquing the gyros. The fine align mode is actually a gyro torquing function accomplished during the inertial reference mode. The torquing current to the gyros is provided by the fine align electronics located in the PTA. The fine align electronics is enabled and controlled by LGC pulses sent directly to the fine align electronics. The LGC does not send command discretes to the ISS CDU's during this mode. The ISS is in the inertial reference mode prior to the enabling of the fine align electronics and returns to that mode when the fine align electronics is disabled.

The fine align electronics torques the gyros on a time shared basis. The LGC sends four types of pulse trains to the fine align electronics. The first pulse train sent is the torque enable command which enables the fine align electronics. The second pulse train is a gyro select command which selects a particular gyro and the direction it is to be torqued by means of a switching network which closes the current path through the proper torque ducosyn coil. The third and fourth types of pulse trains are the torque set and torque reset commands which control a binary current switch to start and stop the current flow through the selected torque ducosyn coil. The amount of current flow through the torque ducosyn coils is precisely controlled at a fixed value. The amount of gyro torquing to be accomplished is determined by the amount of time torque current is applied; that is, the time duration between the receipt of the torque set and the torque reset commands. This time duration is calculated by the LGC. The torque ducosyn displaces the gyro float, causing the ducosyn signal generator to apply an error signal to the stabilization loop. The stabilization loops drive the gimbals to reposition the stable member. Upon completion of the torquing, the stable member remains fixed in its inertial reference and in fine align mode until the torque enable command is removed, after which the ISS remains in inertial reference mode until further change is commanded.

During the fine align mode, the ISS CDU error counters remain cleared and inhibited. The CDU read counters continue to repeat the gimbal angles and send angular data ± $(\Delta\theta_G)$ to the LGC.

2-4.5.8 Attutide Error Indication. The attitude error indication mode supplies attitude error signals to the FDAI. The attitude error indication mode is initiated when the LGC sends the ISS error counter enable discrete to the CDU. The LGC will calculate the difference between the actual gimbal angles and the correct angles and convert this into the number of $\pm \Delta\theta_c$ pulses to be sent to the error counter. The error counter, having been enabled, accepts the pulses and counts up or down until it has registered all the pulses.

The digital information in the error counter is converted into an 800 cps, amplitude modulated, analog error signal by the ladder decoder in the D/A converter. This ac signal is applied through a scaling amplifier to the FDAI. As the actual gimbal angles change, the LGC sends additional $\pm \Delta\theta_c$ pulses to count the error counter up or down, thereby changing the signal to the FDAI.

2-4.5.9 Display Inertial Data. The display inertial data mode permits the LGC to provide inertially derived forward and lateral velocity signals through the digital to analog section of the RR channels of the CDU to the LEM velocity display meters. The display inertial data mode is used during the last phases of the LEM powered descent.

The display inertial data mode is requested by the astronaut closing a switch on the main control panel. (See figure 2-16.) The mode is initiated by the LGC sending the display inertial data discrete to the RR channels of the CDU. The display inertial data discrete acts through a relay driver to energize relays which connect the D/A converter dc error signal outputs to the LEM velocity display meters. After a brief delay to allow for relay pull in time, the LGC sends the D/A enable discrete followed by incrementing pulses to the error counters. The LGC sends $\pm\Delta\theta_c$ pulses representing LEM forward velocity (motion along the Z_{LEM} axis) to one error counter and $\pm\Delta\theta_c$ pulses representing LEM lateral velocity (motion along the vehicle Y_{LEM}) to the other error counter. The read counters will not send incrementing pulses to the error counters; therefore, the only information registered in the error counters will be the $\pm\Delta\theta_c$ pulses.

The digital information registered in the error counter is converted into an 800 cps, amplitude modulated, analog signal by the ladder decoder in the D/A converter. This signal is converted into a dc analog signal by a phase sensitive demodulator circuit also located in the D/A converter. The dc analog signal is applied through the energized relay contacts to the LEM velocity display meters. As the velocity changes, as calculated by the LGC, representative $\pm\Delta\theta_c$ pulses will continue to be sent to the error counter, causing it to count up or down and thereby changing the D/A converter dc signal to the display meters.

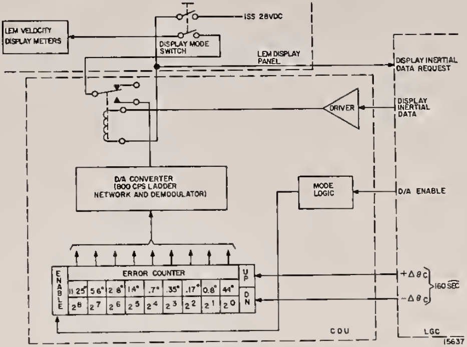


Figure 2-16. Display Inertial Data Mode

2-4.5.10 Master Reset Condition (Test Area Only). The purpose of the master reset condition is to establish preselected standard operating modes in both the airborne equipment and the GSE. The master reset condition is operable in the ISS test configuration only. The master reset condition is initiated when the MASTER RESET pushbutton on the test control panel of the OIA is pressed.

The effects of establishing a master reset condition are dependent upon the particular ISS level of test, power mode status, et cetera, at the time the MASTER RESET pushbutton is pressed. With the ISS STANDBY pushbutton selected, but prior to pressing the ISS OPERATE pushbutton, the MASTER RESET pushbutton will cause the simultaneous closure of the IMU stabilization loops. During the first 90 seconds after pressing the ISS OPERATE pushbutton, the MASTER RESET pushbutton is disabled. Ninety seconds after pressing the ISS OPERATE pushbutton, the MASTER RESET pushbutton is enabled and, if selected, simultaneously performs the following operations: causes the coarse align mode to be commanded, places the gimbals under gimbal positioner control, and removes all IMU caging signals. The master reset condition also discontinues all RR mode commands and commands the RR channels of the CDU to repeat the RR angles.

2-4.6 ISS POWER SUPPLIES.

The ISS power supplies convert the +28 vdc prime LEM power into the various dc and ac voltages required by the ISS. The power supplies are the pulse torque power supply; the -28 vdc power supply; the 800 cps, 1 percent power supply; the 800 cps, 5 percent, 2 phase, power supply; and the 3,200 cps power supply. The pulse torque power supply is in the PTA and the remaining power supplies are in the PSA.

The +28 vdc prime power is supplied by the LEM electrical power system through the ISS OPERATE circuit breaker. All ac power supplies are synchronized to the LGC clock by means of computer pulses. The dc supplies, using multivibrators as ac sources for transformation, are also synchronized to the LGC. Synchronization is accomplished by a multivibrator which will free run at a lower frequency without the computer pulses, assuring operation of the ISS power supplies in the event of an LGC failure.

2-4.6.1 Pulse Torque Power Supply. The pulse torque power supply (figure 2-17) provides 120 vdc to the three binary current switches and three dc differential amplifiers in the accelerometer loops and the binary current switch and dc differential amplifier in the stabilization loop fine align electronics. The pulse torque power supply also provides three individual 28 vdc outputs to the accelerometer loop PVR's, 20 vdc to the three accelerometer loop ac differential amplifier and interrogator modules and the associated binary current switches, and -20 vdc to the ac differential amplifier and interrogator module in the accelerometer loops.

The -20 vdc output is derived from the -28 vdc power supply by using a zener diode as a voltage divider and regulator. The output is regulated at -20(±0.8) vdc.

The 20 vdc output is derived from 28 vdc prime power by the use of a three transistor series regulator which maintains the output voltage at 20 (±0.55) vdc.

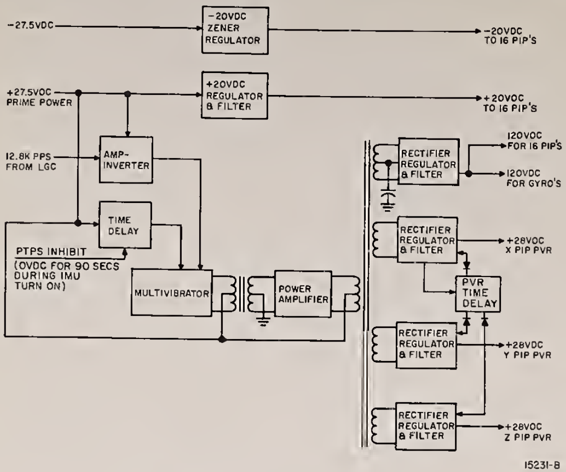


Figure 2-17. Pulse Torque Power Supply

The 120 vdc and 28 vdc PVR outputs are derived from a multivibrator, a power amplifier, and a rectifier and filter. A 12.8 kpps synchronizing pulse is received from the LGC through a buffer transformer in the pulse torque insolation transformer assembly and is applied to an amplifier-inverter. The output of the amplifier-inverter is applied to a multivibrator-chopper causing it to be synchronized at 6,400 cps. A transistorized time delay circuit is incorporated into the emitter circuits of the multivibrator to provide a turn on time delay of approximately 350 milliseconds. During the 90 second IMU turn on mode, 0 vdc is applied through the turn on circuits of the IMU auxiliary assembly module to the time delay circuit which inhibits the 120 vdc and

28 vdc PVR supplies. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a two stage push-pull power amplifier which operates from 28 vdc prime power. The output of the power amplifier consists of a transformer with four secondary windings; one with center tap return for the 120 vdc power supply, and one each for the X, Y, and Z accelerometer loop 28 vdc PVR supplies. The 120 vdc power supply consists of a full wave rectifier whose output is filtered, regulated, and again filtered. The 28 vdc power supplies are identical and consist of a full wave bridge rectifier whose output is filtered, regulated, and again filtered. The PVR time delay circuit inhibits the operation of the regulator in each 28 vdc PVR circuit to provide a six to eight second time delay in the 28 vdo PVR outputs.

2-4.6.2 -28 VDC Power Supply. The -28 vdc power supply provides input power to the three gimbal servo amplifiers in the stabilization loops and to the pulse torque power supply to generate -20 vdc for use in the accelerometer loops. The -28 vdc power supply consists of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, and a rectifier and filter. (See figure 2-18.) The 25.6 kpps synchronization pulse input is amplified and inverted for use in synchronizing the multivibrator-chopper at 12.8 kcps. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a push-pull power amplifier. The output of the amplifier is transformer coupled to a full wave rectifier and filter whose positive side is referenced to ground to provide a -27.0 (±1.0) vdc output.

2-4.6.3 800 CPS Power Supply. The 800 cps power supply (figure 2-19) consists of four modules: an automatic amplitude control, filter, and multivibrator; a 1 percent amplifier; and two 5 percent amplifiers. The 1 percent amplifier provides IMU gimbal resolver excitation, gimbal servo amplifier demodulator reference, and FDAI and control electronics section (CES) reference. The two 5 percent amplifiers provide gyro wheel excitation, IMU blower excitation, and accelerometer fixed heater power. The 1 percent amplifier also provides the input to one of the 5 percent amplifiers whose output is phase shifted -90 degrees. The output of this 5 percent amplifier is applied to the second 5 percent amplifier whose output is also phase shifted -90 degrees, or -180 degrees from the output of the 1 percent amplifier. The outputs of the 1 percent amplifier and the 5 percent amplifiers are applied to their respective loads through the IMU load compensation network which provides a power factor correction.

Zero and pi phase, 800 cps pulse trains from the LGC synchronize the multivibrator at 800 cps. In the absence of the synchronizing pulses, the multivibrator will free run between 720 and 790 cps. The output of the multivibrator controls the operation of the chopper and filter circuit. The filtered chopper output is applied to the 1 percent amplifier. The output of the 1 percent amplifier, in addition to its direct uses, is a feedback signal to the automatic amplitude control circuit. The positive peaks of this feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the multivibrator driven chopper. The bias controls the amplitude of the chopped signal.

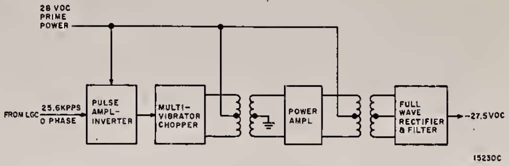


Figure 2-18. -28 VDC Power Supply

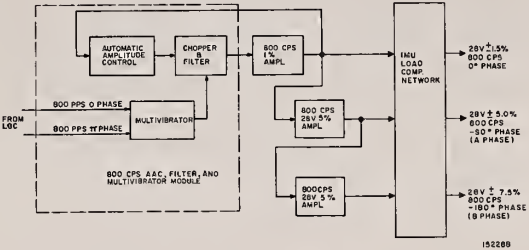


Figure 2-19. 800 CPS Power Supply

The 1 percent amplifier is push-pull in operation with transformer coupled input and output and with overall voltage feedback for gain and distortion control.

The two 5 percent amplifiers are identical in operation. The amplifiers are push-pull and have transformer coupled inputs and outputs. The input transformer primary center tap is connected to the input signal low. The input signal high is applied directly to one side of the primary winding and is also applied through a phase shift network to the other, or out of phase, side of the primary. A feedback signal from the secondary of the output transformer is also applied to the out of phase side of the input transformer primary where it is mixed with the phase shifted portion of the input signal. This mixing results in a -90 degree phase shift in the secondary of the input transformer. The output of the first 5 percent amplifier is used as an input to the second 5 percent amplifier to provide an additional -90 degree phase shift.

2-4.6.4 3,200 CPS Power Supply. The 3,200 cps power supply provides excitation voltage for the signal generator and the magnetic suspension portions of the IRIG and PIP ducosyns. The 3,200 cps output is also used as a reference for the demodulator in the gimbal servo amplifiers.

The excitation voltage to the signal generators requires both voltage stability and phase stability. To accomplish this stability, the excitation voltage power transmission to the stable member is through a step down transformer on the stable member which reduces the slip ring current and, therefore, voltage drop effects due to slip ring, cable, and connector resistance. In addition, each wire connecting the output of the transformer to the input terminals of each PIP is cut to exactly the same length. The voltage level at the primary of the transformer is fed back to the power supply and is compared to a voltage reference.

The 3,200 cps power supply (figure 2-20) consists of an amplitude control module and a 1 percent power amplifier. The amplitude control module contains an automatic amplitude control circuit, a multivibrator, a chopper, and a filter.

The 3,200 pps pulse trains of zero degree phase and 180 degree phase synchronize a multivibrator. The output of the multivibrator controls the operation of the chopper circuit. The output of the chopper is applied to the 1 percent power amplifier. The 28 volt rms output of the amplifier is transmitted through the slip rings to the transformer on the stable member where the voltage is stepped down to 2 volts for the accelerometer ducosyns and 4 volts for the gyro ducosyns. A sample of the 28 volt level at the primary of the transformer is fed back through the slip rings to the input of the automatic amplitude control circuit. The positive peaks of the feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the chopper circuit. The dc bias controls the amplitude of the chopper output to the filter.

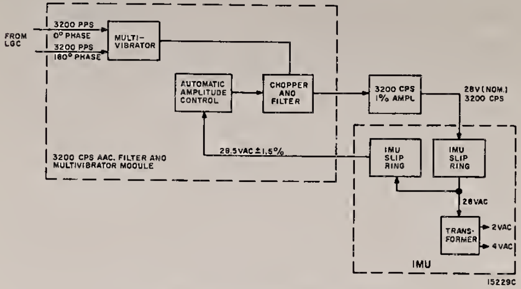


Figure 2-20. 3,200 CPS Power Supply

2-5 ALIGNMENT OPTICAL TELESCOPE

The AOT provides a means of manually taking direct visual sightings and precision angular measurements of preselected celestial targets. These measurements are manually transferred by the astronaut to the LGC through the DSKY. The LGC uses this angular information along with pre-stored data to compute the LEM position and velocity and to accomplish a fine alignment of the IMU stable member.

In the lunar pre-launch phase, the AOT is used to obtain the necessary information for an accurate LEM launch trajectory to intercept the CSM.

During lunar orbital flight, the measurements obtained with the AOT are used by the LGC to define the vehicle's position, and to correct vehicle velocity for the desired lunar orbital or landing trajectory.

2-5.1 LUNAR PRE-LAUNCH MODE. The primary function of the AOT is to facilitate an accurate determination of the vehicle's position and to fine align the IMU stable member, in an inertial coordinate reference system, prior to launch from the lunar surface. The AOT is first positioned (manually) to one of three viewing detents to make the preselected target visible within the 60 degree field of view. The AOT is then manually adjusted to obtain angular measurements, referenced to the nav base, of the target's position in shaft and trunnion. The angular measurements are read out by the astronaut from a mechanical counter on the AOT and manually entered into the LGC through the DSKY. After angular measurements are made on two separate targets and data fed into the LGC, the LGC updates the computation of the LEM position. Using the star framework as a reference, the LGC then aligns the IMU stable member.

2-5.2 LUNAR ORBITAL FLIGHT MODE. In lunar orbital flight, the AOT is manually set to the center forward viewing detent. The LEM attitude is then changed by the astronaut until the target image is within the AOT field of view and the vehicle limit cycle causes the image to appear to oscillate across the reticle X and Y crosshairs. As the target image crosses the X or Y crosshair, the astronaut markes the time of each crossing by manually keying the LGC through the MARK X or MARK Y push-button on the computer control and reticle dimmer assembly (CCRD). This procedure is then repeated using another target star. The LGC utilizes the crossing time inputs and the LEM attitude angles to compute the LEM velocity and improve the accuracy of the estimate of the LEM position. The LGC then fine aligns the IMU and fires the necessary RCS jets to increase or decrease velocity for the projected lunar orbital and landing trajectory.

2-6 COMPUTER SUBSYSTEM

The computer subsystem (CSS) is the control and processing center of the PGNCS. It consists of the LGC and a DSKY. The CSS processes data and issues discrete outputs and control pulses to the PGNCS and other LEM systems. The LGC is a parallel digital control computer with many features of a general purpose computer. As a control computer, the LGC aligns the IMU, positions the RR antenna and issues control commands to other LEM systems. As a general purpose computer, the LGC solves the guidance and navigation equations required for the LEM mission. In addition, the LGC monitors the operation of the LEM, including the CSS.

The main functions of the LGC (see figure 2-21) are implemented through the execution of the programs stored in memory. Programs are written in a machine language called basic instructions. A basic instruction contains an operation (order) code and a relevant address. The order code defines the data flow within the LGC, and the relevant address selects the data that is to be used for computations. The order code of each instruction is entered into the sequence generator, which controls data flow and produces a different sequence of control pulses for each instruction. Each instruction is followed by another instruction. In order to specify the sequence in which consecutive instructions are to be executed, the instructions are normally stored in successive memory locations. By adding the quantity one to the address of an instruction being executed, the address of the instruction to be executed next is derived. Execution of an instruction is complete when the order code of the next instruction is transferred to the sequence generator and the relevant address is in the central processor.

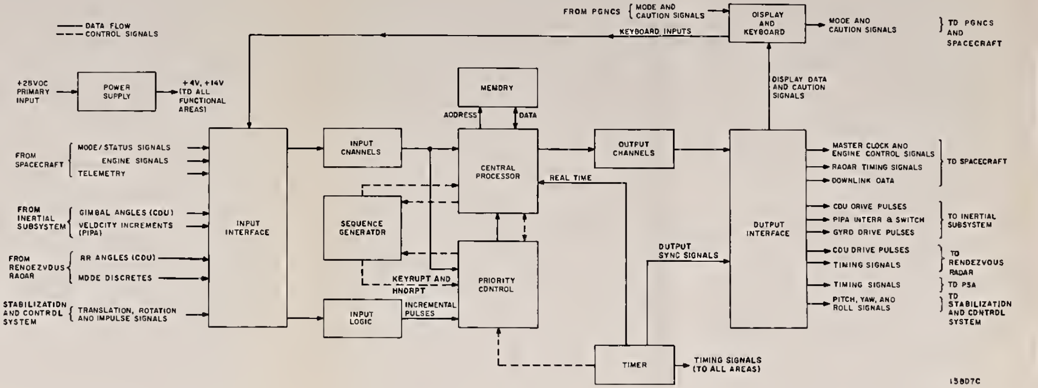


Figure 2-21. Computer Subsystem, Block Diagram

The central processor consists of several flip-flop registers. It performs arithmetic operations and data manipulations on information accepted from memory, the input channels, and priority control. Arithmetic operations are performed using the ONE's complement number system. Values of 14 bits, excluding sign, (up to 28 bits during double precision operations) are processed with an additional bit produced for overflow or underflow. All operations within the central processor are performed under control of pulses generated by the sequence generator (indicated by dashed lines in figure 2-21). In addition, all words read out of memory are checked for correct parity, and a parity bit is generated within the central processor for all words written into memory. The LGC uses odd parity, that is, all words stored in memory contain an odd number of ONE's including the parity bit. The central processor also supplies data and control signals through the output channels and provides interface for the various spacecraft subsystems.

The LGC has ten program interrupt conditions. These ten interrupts are T6 RUPT, T5 RUPT, T3 RUPT, T4 RUPT, KYRPT 1, KYRPT 2 (or MKRPT), UPRUPT, DLKRPT, RADRPT, and HNDRPT. The T6 RUPT through T4 RUPT conditions are internal interrupts initiated by the LGC. The KYRPT 1 condition is initiated when a DSKY pushbutton is depressed. A MARK signal (discrete bit), indicating a sighting, initiates KYRPT 2. This interrupt shares the same priority as the KYRPT 2 interrupt associated with the navigation DSKY in the CSM application of the computer. UPRUPT indicates the completion of an uplink word. RADRPT is generated when a complete radar word is received. HNDRPT is initiated as soon as the hand controller is moved out of detent by the astronaut.

Before a priority program can be executed, the current program must be interrupted; however, certain information about the current program must be preserved. This information includes the program counter contents and any intermediate results contained in the central processor. The priority control produces an interrupt request signal, which is sent to the sequence generator. This signal, acting as an order code, causes the execution of an instruction that transfers the current contents of the program counter and any intermediate results to memory. In addition, the control pulses transfer the priority program address in priority control to the central processor, and then to memory through the write lines. As a result, the first basic instruction word of the priority program is entered into the central processor from memory, and execution of the priority program is begun. The last instruction of each priority program restores the LGC to normal operation, provided no other interrupt request is present, by transferring the previous program counter and intermediate results from their storage locations in memory back to the central processor.

Certain data pertaining to the flight of the LEM is used to solve the guidance and navigation problems required for the LEM mission. This data, which includes real time, acceleration, and IMU gimbal angles, is stored in memory locations called counters. The counters are updated as soon as new data becomes available. An incrementing process which changes the contents of the counters is implemented by priority control between the execution of basic instructions. Data inputs to priority control are called incremental pulses. Each incremental pulse produces a counter address and a priority request. The priority request signal is sent to the sequence generator, where it functions as an order code. The control pulses produced by the sequence generator transfer the counter address to memory through the write lines of the central processor. In addition, the control pulses enter into the central processor the contents of the addressed counter to be incremented.

Real time plays a major role in solving guidance and navigation problems. Real time is maintained within the LGC in the main time counter of memory. The main time counter provides a 745.65 hour (approximately 31 days) clock. Incremental pulses are produced in the timer and sent to priority control for incrementing the main time counter. The LEM mission requires that the LGC clock be synchronized with the KSC clock. The LGC time is transmitted once every second by downlink operation for comparison with the KSC clock.

Incremental transmissions occur in the form of pulse bursts from the output channels to the CDU, the gyro fine align electronics, the RCS of the spacecraft, the optical tracker and the radar. The number of pulses and the time at which they occur are controlled by the LGC program. Discrete outputs also originate in the output channels under program control. These outputs are sent to the DSKY and various other subsystems. Continuous pulse trains originate in the timing output logic for synchronization of other systems.

The uplink word from the LEM telemetry system (unmanned flights) is supplied as an incremental pulse input to priority control. As this word is received, priority control procudes the address of the uplink counter in memory and requests the sequence generator to execute the instructions which perform the serial-to-parallel conversion of the input word. When the serial-to-parallel conversion is completed, the parallel word is transferred to a storage location in memory by the uplink priority program. The uplink program also retains the parallel word for subsequent downlink transmission. Another program converts the parallel word to a coded display format and transfers the display information to the DSKY.

The downlink operation of the LGC is asynchronous with respect to the LEM telemetry system. The telemetry system supplies all the timing signals necessary for the downlink operation. These signals include start, end, and bit sync pulses.

Through the DSKY, the astronaut can load information into the LGC, retrieve and display information contained in the LGC, and initiate any program stored in memory. A keycode is assigned to each keyboard pushbutton. When a keyboard pushbutton on the DSKY is depressed, the keycode is produced and sent to an input channel. A signal is also sent to priority control, where it produces both the address of a priority program stored in memory and a priority request signal, which is sent to the sequence generator. This operation results in an order code and initiates an instruction for interrupting the program in progress and executing the KEYRUPT priority program stored in memory.

A function of this program is to transfer the keycode, temporarily stored in an input channel, to the central processor, where it is decoded and processed. A number of keycodes are required to specify an address, or a data word. The program initiated by a keycode also converts the information from the DSKY keyboard to a coded display format. The coded display format is transferred by another program to an output channel and sent to the display portion of the DSKY. The display notifies the astronaut that the keycode was received, decoded, and processed properly by the LGC.

2-6.1 PROGRAMS. An LGC program performs such functions as solving guidance and navigation problems, testing the operation of the PGNCS, and monitoring the operation of the LEM. Such a program consists of a group of program sections that are classified according to the functions they perform. These functions are defined as mission functions, auxiliary functions, and utility functions. (See figure 2-22.)

2-6.1.1 Mission Functions. Mission functions are performed by program sections that implement operations concerned with the major objectives of the LEM mission. These operations include erecting the IMU stable member and coarse aligning it to a desired heading prior to separating the LEM from the CSM and fine aligning it after separation. In addition, the mission functions include computation of spacecraft position and velocity during coasting periods of the flight by solution of second-order differential equations which describe the motions of a body subject to the forces of gravity.

2-6.1.2 Auxiliary Functions. Auxiliary functions are executed at the occurrence of certain events, requests, or commands. These functions are performed by program sections that provide a link between the LGC and other elements of the PGNCS. This link enables the LGC to process signals from various devices and to send commands for control and display purposes. In addition, the auxiliary functions implement many and varied operations within the LGC in support of the LEM mission functions.

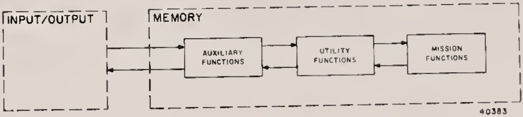


Figure 2-22. Program Organization

2-6.1.3 Utility Functions. Utility functions are performed by program sections that coordinate and synchronize LGC activities to guarantee orderly and timely execution of required operations. These functions control the operation of the LEM mission functions and schedule LGC operations on either a priority or a real-time basis. The utility functions also translate interpretive language to basic machine language which allows complex mathematical operations such as matrix multiplication, vector addition, and dot product computations to be performed within the framework of compact routines. In addition, the utility functions save the contents of registers A and Q during an interrupt condition and enable data retrieval and control transfer between isolated banks in the fixed-switchable portion of fixed memory.

2-6.2 MACHINE INSTRUCTIONS. The LGC has three classes of machine instructions: regular, involuntary, and peripheral (table 2-I). Regular instructions are programmed and are executed in whatever sequence they have been stored in memory. Involuntary instructions (with one exception) are not programmable and have priority over regular instructions. One involuntary instruction may be programmed to test computer operations. No regular instruction can be executed when the LGC forces the execution of an involuntary instruction. The peripheral instructions are used when the LGC is connected to the peripheral equipment. During the execution of any peripheral instruction, the LGC is in the monitor stop mode and cannot perform any program operation.

2-6.2.1 Regular Instructions. Four types of instructions comprise the regular instruction class. They are the basic, channel, extracode, and special instructions. Basic instructions are used most frequently. The instruction words stored in memory are called basic instruction words. They contain an order code field and an address field. Special instructions have predefined addresses and order codes; basic instructions have only predefined order codes. The special instructions are used to control certain operations in the LGC. For example, one special instruction is used to switch the LGC to the extend mode of operation. This mode extends the length of the order code field and converts basic instruction words to channel or extracode instruction words. Channel instructions can only be used with input-output channel addresses. Extra code instructions perform the more complex and less frequently used arithmetic operations.

Regular instructions can also be functionally subdivided into the following:

(1) Sequence changing.

(2) Fetching and storing.

(3) Modifying.

(4) Arithmetic and logic.

(5) Input-output.

(6) Editing.

Table 2-I. Instruction Classes

Class	Type	Control
Regular	Basic Extracode Channel Special	Program
Involuntary	Interrupt Counter	Priority
Peripheral	Keyboard Tape	Operator

The sequence changing instructions alter the sequence in which the instructions stored in memory are executed. One group, called transfer control instructions, changes the program path as defined by the programmer. The other group, called decision making instructions, branches to alternate program paths in response to predefined conditions.

The fetching and storing instructions move data, without alteration, from one location to another. One group, called copy instructions, provides a non-destructive transfer of data from memory to the central processor. Another group, called exchange instructions, transposes data between memory and the central processor. One instruction provides a nondestructive transfer of data from the central processor to memory.

The modifying instructions alter the next instruction to be executed by changing the contents of the order code field, address field, or both.

The arithmetic and logic instructions perform numerical computations. One group, called the basic arithmetic instructions, performs addition, subtraction, multiplication, and division in the ONE's complement number system. Another group, called the add and store instructions, performs single or double precision addition and transfers the resultant from the central processor to memory. The incrementing instructions increment a signed quantity, increment its absolute value, or diminish its absolute value by one. One instruction performs subtraction in the TWO's complement number system for angular data and one instruction performs the Boolean AND operation.

The input-output or channel instructions link the interface circuits to the central processor. One group, called read instructions, transfers the total or partial contents of any channel (register) location to the central processor either directly or accompanied by the Boolean AND, OR, or EXCLUSIVE OR operation. Another group of instructions transfers all new or partially new information to any channel location in the same manner.

The editing or special instructions are address-dependent and control the operation of the program. One special instruction, as mentioned previously, controls the extend mode of operation. Other instructions prevent a program from being interrupted or shift and cycle data to the left or right.

2-6.2.2 Involuntary Instructions. Involuntary instructions contain two types of instructions: interrupt and counter. The interrupt instructions use the basic instruction word format just as the regular instructions do; however, the interrupt instructions are not entirely programmable. The contents of the order code field and the address field are supplied by computer logic rather than the program. The counter instructions have no instruction word format. Signals which function as a decoded order code specify the counter instruction to be executed and the computer logic supplies the address. The address for these instructions is limited to one of 29 counter locations in memory.

There are two interrupt instructions. One instruction initializes the LGC when power is first applied and when certain program traps occur. The other interrupt instruction is executed at regular intervals to indicate time, receipt of new telemetry or keyboard data, or transmission of data by the LGC. This interrupt instruction may be programmed to test the computer.

There are several counter instructions. Two instructions will either increment or decrement by one the content of the counter location using the ONE's complement number system. Two other instructions perform the same function using the TWO's complement number system. Certain counter instructions control output rate signals and convert serial telemetry data to parallel computer data.

2-6.2.3 Peripheral Instructions. There are two types of peripheral instructions. One type deals with memory locations and the other type deals with channel locations. The peripheral instructions are not used when the LGC is in the LEM. They are used when the computer is connected to peripheral equipment during subsystem and preinstallation system testing. The peripheral instructions are not programmable and are executed when all computer program operations have been forcibly stopped. These instructions are used to read and load any memory or channel location and to start the computer program at any specified address. The peripheral instructions and counter instructions are processed identically.

2-6.3 TIMER. The timer generates the timing signals required for operation of the LGC and is the primary source of timing signals for all LEM systems.

The timer is divided into the areas indicated in figure 2-23. The master clock frequency is generated by an oscillator and is applied to the clock divider logic. The divider logic divides the master clock input into gating and timing pulses at the basic clock rate of the computer. Several outputs are available from the scaler, which further divides the divider logic output into output pulses and signals which are used for gating, for generating rate signal outputs, and for accumulating time. Outputs from the divider logic also drive the time pulse generator which produces a recurring set of time pulses. This set of time pulses defines a specific interval (memory cycle time) in which access to memory and word flow take place within the computer.

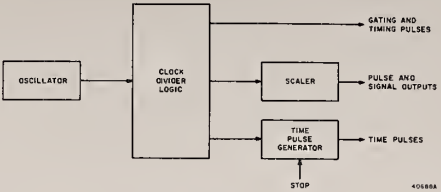


Figure 2-23. Timer, Block Diagram

The start-stop logic senses the status of the power supplies and specific alarm conditions in the computer and generates a stop signal which is applied to the time pulse generator to inhibit word flow. Simultaneous with the generation of the stop signal, a fresh start signal is generated which is applied to all functional areas in the computer. The start-stop logic and subsequent word flow in the computer can also be controlled by inputs from the Computer Test Set (CTS) during pre-installation systems and subsystem tests.

2-6.4 SEQUENCE GENERATOR. The sequence generator executes the instructions stored in memory. The sequence generator processes instruction codes and produces control pulses which regulate the data flow of the computer. The control pulses are responsible for performing the operations assigned to each instruction in conjunction with the various registers in the central processor and the data stored in memory.

The sequence generator (figure 2-24) consists of the order code processor, command generator, and control pulse generator. The sequence generator receives order code signals from the central processor and priority control. These signals are coded by the order code processor and supplied to the command generator. The special purpose control pulses are used for gating the order code signals into the sequence generator at the end of each instruction.

The command generator receives instruction signals from priority control and peripheral equipment and receives coded signals from the order code processor. The command generator decodes the input signals and produces instruction commands which are supplied to the control pulse generator.

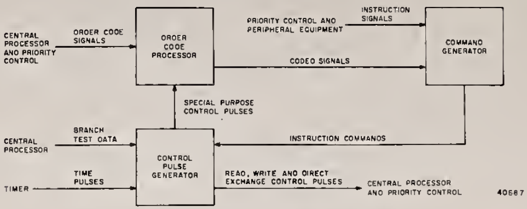

CENTRAL PROCESSOR AND PRIORITY CONTROL
ORDER CODE SIGNALS
ORDER CODE PROCESSOR
PRIORITY CONTROL AND PERIPHERAL EQUIPMENT
INSTRUCTION SIGNALS
COMMAND GENERATOR
CODED SIGNALS
SPECIAL PURPOSE CONTROL PULSES
CENTRAL PROCESSOR
BRANCH TEST DATA
INSTRUCTION COMMANDS
CONTROL PULSE GENERATOR
TIMER
TIME PULSES
READ, WRITE AND DIRECT EXCHANGE CONTROL PULSES
CENTRAL PROCESSOR AND PRIORITY CONTROL
40687

Figure 2-24. Sequence Generator, Block Diagram

The control pulse generator receives twelve time pulses from the timer. These pulses occur in cycles and are used for producing control pulses in conjunction with the instruction commands. There are five types of control pulses: read, write, test, direct exchange, and special purpose. Information in the central processor is transferred from one register to another by the read, write, and direct exchange control pulses. The special purpose control pulses regulate the operation of the order code processor. The test control pulses are used within the control pulse generator. The branch test data from the central processor changes the control pulse sequence of various instructions.

2-6.5 CENTRAL PROCESSOR. The central processor, figure 2-25, consists of the flip-flop registers, the write, clear, and read control logic, write amplifiers, memory buffer register, memory address register, and decoder and the parity logic. All data and arithmetic manipulations within the LGC take place in the central processor.

Primarily, the central processor performs operations indicated by the basic instructions of the program stored in memory. Communication within the central processor is accomplished through the write amplifiers. Data flows from memory to the flip-flop registers or vice-versa, between individual flip-flop registers, or into the central processor from external sources. In all instances, data is placed on the write lines and routed to a specific register or to another functional area under control of the write, clear, and read logic. This logic section accepts control pulses from the sequence generator and generates signals to read the content of a register onto the write lines and to write this content into another register of the central processor or to another functional area of the LGC. The particular memory location is specified by the content of the memory address register. The address is fed from the write lines into this register, the output of which is decoded by the address decoder logic. Data is subsequently transferred from memory to the memory buffer register. The decoded address outputs are also used as gating functions within the LGC.

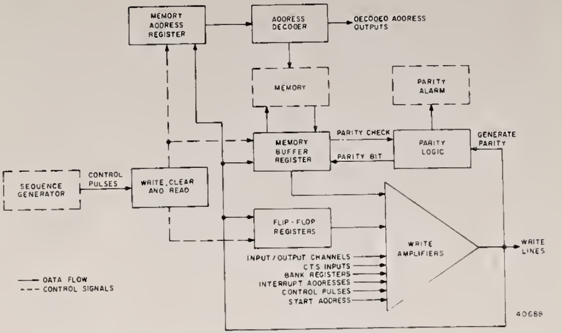


Figure 2-25. Central Processor, Block Diagram

The memory buffer register buffers all information read out or written into memory. During readout, parity is checked by the parity logic and an alarm is generated in case of incorrect parity. During write-in, the parity logic generates a parity bit for information being written into memory. The flip-flop registers perform the data manipulations and arithmetic operations. Each register is 16 bits or one computer word in length. Data flows into and out of each register as dictated by control pulses associated with each register. The control pulses are generated by the write, clear, and read control logic.

External inputs through the write amplifiers include the content of both the erasable and fixed memory bank registers, all interrupt addresses from priority control, control pulses which are associated with specific arithmetic operations, and the start address for an initial start condition. Information from the input and output channels is placed on the write lines and routed to specific destinations either within or external to the central processor. The CTS inputs allow a word to be placed on the write lines during system and subsystem tests.

2-6.6 PRIORITY CONTROL. Priority control is related to the sequence generator in that it controls all involuntary or priority instructions. The priority control processes input-output information and issues order code and instruction signals to the sequence generator and issues twelve-bit addresses to the central processor.

The priority control (figure 2-26) consists of the start, interrupt, and counter instruction control circuits. The start instruction control initializes the computer if the program works itself into a trap, if a transient power failure occurs, or if the interrupt instruction control is not functioning properly. The computer is initialized with the start order code signal, which not only forces the sequence generator to execute the start instruction, but also resets many other computer circuits. When the start order code signal is being issued, the T12 stop signal is sent to the timer. This signal stops the time pulse generator until all essential circuits have been reset and the start instruction has been forced by the sequence generator. The computer may also be initialized manually when connected to the peripheral equipment and placed into the monitor stop mode. In this mode, the time pulse generator is held at the T12 position until the monitor stop signal is released.

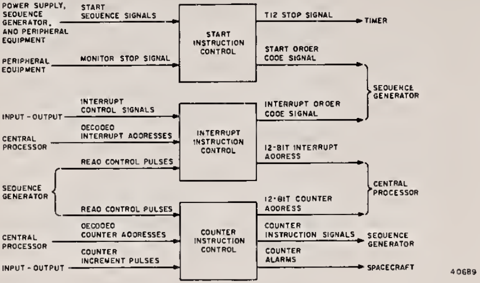


Figure 2-26. Priority Control, Block Diagram

The interrupt instruction control can force the execution of the interrupt instruction by sending the interrupt order code signal to the sequence generator and the twelve bit address to the central processor. There are ten addresses, each of which accounts for a particular function that is regulated by the interrupt instruction control. The interrupt instruction control links the keyboard, telemetry, and time counters to program operations. The interrupt addresses are transferred to the central processor by read control pulses from the sequence generator. The source of the keyboard, telemetry, and time counter inputs is the input-output circuits. The interrupt instruction control has a built-in priority chain which allows sequential control of the ten interrupt addresses. The decoded interrupt addresses from the central processor are used to control the priority operation.

The counter instruction control is similar to the interrupt instruction control in that it links input-output functions to the program. It also supplies twelve-bit addresses to the central processor and instruction signals to the sequence generator. The instruction signals cause a delay (not an interruption) in the program by forcing the sequence generator to execute a counter instruction. The addresses are transferred to the central processor by read control pulses. The counter instruction control also has a built-in priority of the 29 addresses it can supply to the central processor. This priority is also controlled by decoded counter address signals from the central processor. The counter instruction control contains an alarm detector which produces an alarm if an incremental pulse is not processed properly.

2-6.7 INPUT-OUTPUT. The input-output section accepts all inputs to, and routes to other systems all outputs from, the computer. The input-output section (figure 2-27) includes the interface circuits, input and output channels, input logic, output timing logic, and the downlink circuits.

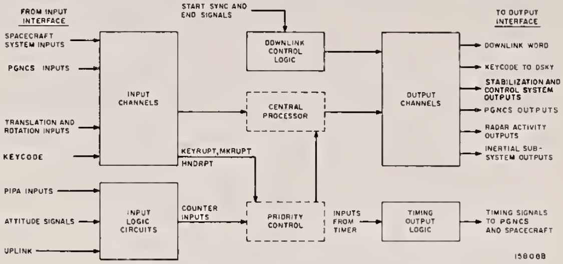


Figure 2-27. Input-Output, Block Diagram

Most of the input and output channels are flip-flop registers similar to the flip-flop registers of the central processor. Certain discrete inputs are applied to individual gating circuits which are part of the input channel structure. Typical inputs to the channels include keycodes from the DSKY and signals from the PGNCS proper and other LEM systems. Input data is applied directly to the input channels; there is no write process as in the central processor. However, the data is read out to the central processor under program control. The input logic circuits accept inputs which cause interrupt sequences within the computer. These incremental inputs (acceleration data from the PIPA's, et cetera) are applied to the priority control circuits and subsequently to associated counters in erasable memory.

Outputs from the computer are placed in the output channels and are routed to specific systems through the output interface circuits. The operation is identical to that in the central processor. Data is written into an output channel from the write lines and readout to the interface circuits under program control. Typically, these outputs include outputs to the stabilization and control system, the DSKY, the PGNCS, et cetera. The downlink word is also loaded into an output channel and routed to the LEM spacecraft telemetry system by the downlink circuits.

The output timing logic gates synchronization pulses (fixed outputs) to the PGNCS and the LEM spacecraft. These are continuous outputs since the logic is specifically powered during normal operation of the computer and during standby.

2-6.8 MEMORY. Memory (figure 2-28) consists of an erasable memory with a storage capacity of 2048 words and a fixed core rope memory with a storage capacity of 36,864 words. Erasable memory is a random-access, destructive-readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a nondestructive storage device. Data stored in fixed memory is unalterable since the data is wired in and readout is nondestructive.

Both memories contain magnetic-core storage elements. In erasable memory, the storage elements form a core array; in fixed memory, the storage elements form three core ropes. Erasable memory has a density of one word per 16 cores: fixed memory has a density of eight words per core. Each word is located by an address.

In fixed memory, addresses are assigned to instruction words to specify the sequence in which they are to be executed; blocks of addresses are reserved for data, such as constants and tables. Information is placed into fixed memory permanently by weaving patterns through the magnetic cores. The information is written into assigned locations in erasable memory with the CTS, the DSKY, uplink, or program operation.

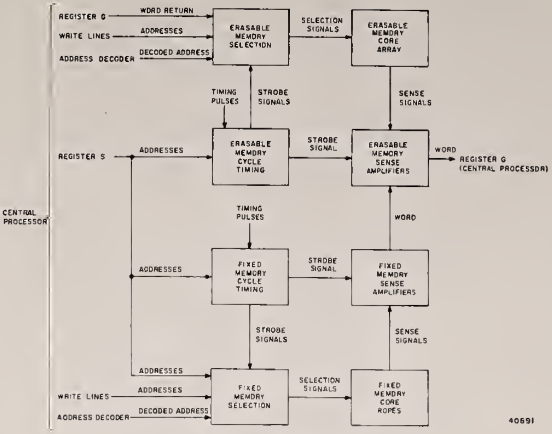


Figure 2-28. Memory, Block Diagram

Both memories use a common address register (register S) and an address decoder in the central processor. When resister S contains an address pertaining to erasable memory, the erasable memory cycle timing is energized. Timing pulses sent to the erasable memory cycle timing then produce strobe signals for the read, write, and sense functions. The erasable memory selection logic receives an address and a decoded address from the central processor and produces selection signals which permits data to be written into or read out of a selected storage location. When a word is read out of a storage location in erasable memory, the location is cleared. A word is written into erasable memory through the memory buffer register (register G) in the central processor by a write strobe operation. A word read from a storage location is applied to the sense amplifiers. The sense amplifiers are strobed and the information is entered into register G of the central processor. Register G receives information from both memories.

The address in register S energizes the fixed memory cycle timing when a location in fixed memory is addressed. The timing pulses sent to the fixed memory cycle timing produce the strobe signals for the read and sense functions. The selection logic receives an address from the write lines, a decoded address and addresses from register S, and produces selection signals for the core rope. The content of a storage location in fixed memory is strobed from the fixed memory sense amplifiers to the erasable memory sense amplifiers and then entered into register G of the central processor.

2-6.9 POWER SUPPLIES. The two power supplies (figure 2-29) furnish operating voltages to the LGC and the DSKY. Primary power of 28 vdc from the spacecraft is applied to both power supplies. Regulator circuits maintain a constant output of +4 volts and +4 volts switched from one supply, and +14 volts and +14 volts switched from the other. The regulator circuits are driven by a sync signal input from the timer, each power supply having a different sync frequency. During system and subsystem tests, inputs from the CTS can be used to simulate power supply failures.

The standby mode of operation is initiated by pressing the standby (STBY) pushbutton on the DSKY. During standby, the LGC is put into a RESTART condition and the switchable +4 and +14 voltages are switched off, thus putting the LGC into a low power mode where only the timer and a few auxiliary signals are operative.

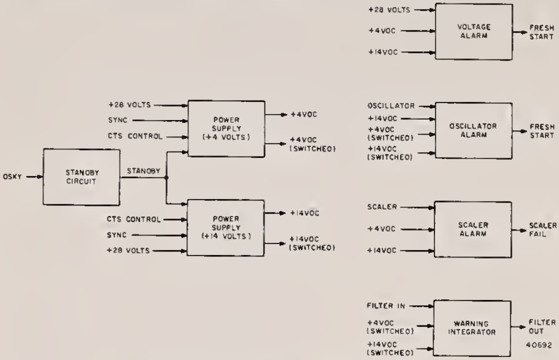


Figure 2-29. Power Supplies, Block Diagram

The voltage alarm circuits monitor the +28, +14, and +4 volt outputs and produce an LGC restart signal (Fresh Start) should any of the voltages deviate from nominal by more than a predetermined amount. The oscillator alarm produces an LGC restart signal (Fresh Start) if the oscillator fails or if the LGC is in the standby mode. The scaler alarm circuit monitors the scaler output of the timer and generates a fail signal if the scaler output fails. The warning integrator monitors certain operations and generates an LGC warning signal (Filter Out) if these operations are frequently repeated or prolonged.

2-6.10 DISPLAY AND KEYBOARD. The DSKY is located below the center panels of the cockpit display and control panels.

The DSKY (figure 2-30) consists of a keyboard; a relay matrix with associated decoding circuits, displays, mode and caution circuits; and a power supply. The keyboard, which contains several numerical, sign, and other control keys, allows the astronaut to communicate with the LGC. The inputs from the keyboard are entered into an input channel and processed by the LGC.

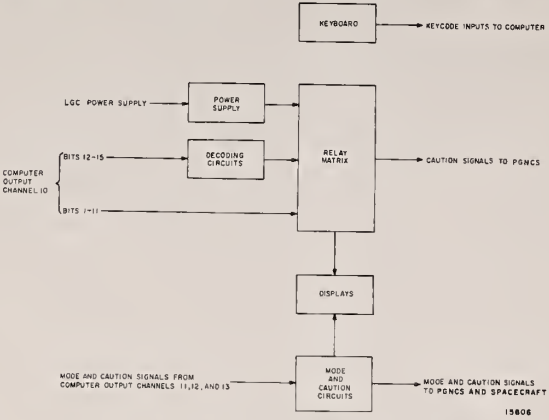

KEYBOARD
KEYCODE INPUTS TO COMPUTER
LGC POWER SUPPLY
POWER SUPPLY
BITS 12-15
DECODING CIRCUITS
RELAY MATRIX
CAUTION SIGNALS TO PGNCS
COMPUTER OUTPUT CHANNEL 10
BITS 1-11
DISPLAYS
MODE AND CAUTION SIGNALS FROM COMPUTER OUTPUT CHANNELS 11,12, AND 13
MODE AND CAUTION CIRCUITS
MODE AND CAUTION SIGNALS TO PGNCS AND SPACECRAFT
15806

Figure 2-30. Display and Keyboard (DSKY), Block Diagram

The inputs entered from the keyboard, as well as other information, appear on the displays after processing by program. The display of information is accomplished through the relay matrix. A unique code for the characters to be displayed is formed by fifteen bits from output channel 10 in the LGC. Bits 12 through 15 are decoded by the decoding circuits, and, along with bits 1 through 11, energize specific relays in the matrix which causes the appropriate characters to illuminate. The information displayed is the result of a keycode punched in by the astronaut, or is computer-controlled information. The display characters are formed by electroluminescent segments which are energized by a voltage from the power supply routed through relay contacts. Specific inputs from the PGNCS are also applied, through the LGC to certain relays in the matrix through output channel 10 of the LGC. The resulting relay-controlled outputs are caution signals to the PGNCS.

The mode and caution circuits accept direct input signals from channels 11, 12, and 13, without being decoded. The resulting outputs can give an indication to the astronaut on the DSKY and route the output signal to the PGNCS and spacecraft.

Chapter 3

PHYSICAL DESCRIPTION

3-1 SCOPE

This chapter describes the physical characteristics of the components which comprise the LEM PGNCS. The locations of the PGNCS components within the LEM are illustrated in figure 3-1.

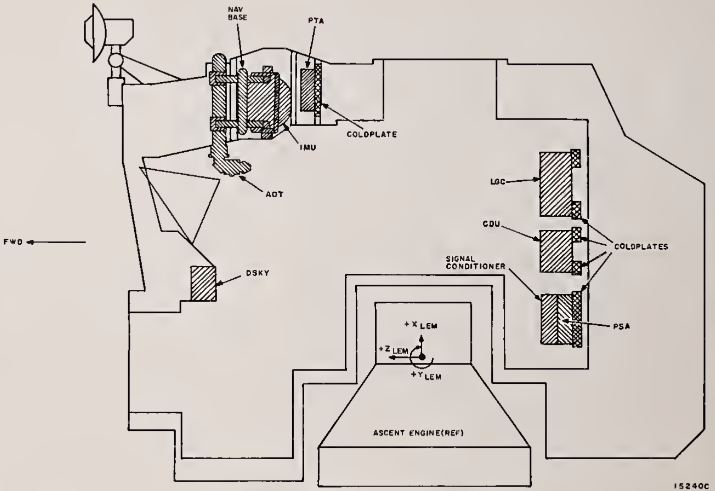


Figure 3-1. Location of LEM PGNCS Components

Chapter 3

PHYSICAL DESCRIPTION

3-1 SCOPE

This chapter describes the physical characteristics of the components which comprise the LEM PGNCS. The PGNCS components and their locations within the LEM are listed in table 3-I and illustrated in figure 3-1. The locations of PGNCS component modules are also illustrated and the module functions described.

3-2 PGNCS INTERCONNECT HARNESS GROUP (LEM)

The PGNCS interconnect harness group (composed of interconnect harnesses A and B) interconnects the components of the PGNCS and provides the electrical interface between the PGNCS and other LEM systems. The IMU and PTA are interconnected by harness B. Harness A interconnects the PSA, CDU, LGC, and signal conditioner. The two harnesses are connected to each other by vehicle cables. Table 3-II lists the harness connectors and the components or cable to which they are mated.

Table 3-I. LEM PGNCS Components

Component	Part Number	Location
AOT	6011000	Mounted on nav base on forward structure of LEM with shaft protruding through top of LEM.
CCRD	6014512	Mounted on bracket on side of AOT eyepiece assembly on PGNCS systems below P/N 6015000-061. Mounted on spacecraft AOT guard assembly on PGNCS systems P/N 6015000-061 and above.
CDU	2007222 2010744	Mounted on coldplate on center section of after crew compartment wall.

(Sheet 1 of 3)

Table 3-I. LEM PGNCS Components

Component	Part Number	Location
PGNCS interconnect harness group (LEM)	6014515	
Interconnect harness A	6014506	Attached to rear wall of after crew compartment.
Interconnect harness B	6014507	Located in IMU compartment.
IMU and PTA	6010747 6007001	
IMU	2018601 2018699	Bolted to after end of nav base.
PTA	6007000 6010656	Mounted on coldplate on LEM structure immediately aft of IMU/nav base complex.
LEM guidance computer group	6003001	
DSKY	2003985	Mounted on front wall of crew compartment below LEM display and control panel.
LGC	2003100	Mounted on coldplate on upper section of after crew compartment wall above CDU.
LGC	2003200	Mounted on coldplate on upper section of after crew compartment wall above CDU.
DSKY	2003950	Mounted on front wall of crew compartment below LEM display and control panel.

(Sheet 2 of 3)

3-1A LEM COMPATIBILITY

Compatibility tables 3-I through 3-IN list the LEM PGNCS components, part numbers, and dash numbers. These tables identify Apollo airborne component configurations and their compatibility to PGNCS applications, and trace Apollo airborne component configuration changes by ECP. The data is organized to assist field site personnel in determining equipment compatibility and to aid in making valid replacement decisions. Table 3-A1 lists the compatibility tables in alphabetical order according to component or assembly. An ECP matrix has also been provided in the table. The matrix is useful for determining which components or assemblies are affected by an ECP.

Table 3-A1. Compatibility and ECP Matrix

ECP Number

Component or Assembly	Table	[illegible]	173	176	179	191	187	204	217	221	236	[illegible]	[illegible]	257	258	259	[illegible]	291	[illegible]	301	302	[illegible]	[illegible]	305	309	310	311	314	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	339	[illegible]	[illegible]	[illegible]
AOT	3-1		x				x												x	x								x	x	x						x			x		
CCku	3-1A																																								
CDU	3-1B	x				x														x													x								
IMU and PTA	3-1C							x		x		x								x		x	x	x	x	x	x										x				
Interconnect harness group	3-1D																																								
LGC group LGC	3-1E			x							x		x	x	x	x				x											x	x			x						x
DSKY	3-1F			x														x																						x	
LGC group installation kit	3-1G																																								
LGC test modules jumper modules	3-1H																																								
rope modules	3-1J																																								
Nav base	3-1K																																	x				x			
PSA	3-1L				x				x								x			x							x														
Signal conditioner assembly (SCA)	3-1M																				x																				
Signal conditioner assembly installation kit	3-1N																																								

Component or Assembly	Table	[illegible]	[illegible]	403	412	[illegible]	421	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	461	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
AOT	3-1				x		x	x					x					x														x					x	x	x	x	
CCku	3-1A							x																												x					
CDU	3-1B	x																									x						x								
IMU and PTA	3-1C	x																										x													
Interconnect harness group	3-1D	x																																	x						x
LGC group LGC	3-1E		x	x					x	x	x	x		x			x		x		x		x	x					x	x	x			x							
DSKY	3-1F					x											x			x		x			x	x			x	x											
LGC group installation kit	3-1G																																								
LGC test modules jumper modules	3-1H																																								
rope modules	3-1J																																								
Nav base	3-1K															x																									
PSA	3-1L	x													x																										
Signal conditioner assembly (SCA)	3-1M																																								
Signal conditioner assembly installation kit	3-1N																																								

Component or Assembly	Table	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	653	[illegible]	[illegible]	673	[illegible]	[illegible]	[illegible]	710	[illegible]	[illegible]	[illegible]	737	[illegible]	[illegible]	741	815	1017 & [illegible]	1010
AOT	3-1				x				x					x					x				x				x							x				
CCku	3-1A							x	x					x																								
CDU	3-1B			x	x					x			x					x																	x			x
IMU and PTA	3-1C					x	x		x			x		x				x			x				x	x											x	
Interconnect harness group	3-1D		x		x				x					x			x																					
LGC group LGC	3-1E			x							x							x										x								x		
DSKY	3-1F																			x				x					x	x			x					
LGC group installation kit	3-1G	x																				x									x							
LGC test modules jumper modules	3-1H																																					
rope modules	3-1J																																					
Nav base	3-1K																																					
PSA	3-1L				x				x					x	x			x														x						
Signal conditioner assembly (SCA)	3-1M				x				x					x		x																						
Signal conditioner assembly installation kit	3-1N																																					

The symbol ① in the compatibility tables depicts an "OR" gate. Follow one path or the other (not both) for entry or exit from gate.

Table 3-I. AOT Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000									SYSTEM SERIAL NUMBERS								
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616	171 / 617	181 / 618
6011000	000	X	T	→	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
	012	T	X	T	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
	031	C	T	C	T	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
	032	C	T	C	X	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
	041	C	T	C	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
	042	C	T	C	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
	071	NO	→	→	→	T	→	→	→	→	→	→	→	→	→	→	→	→	→
	072	NO	→	→	→	T	→	→	→	→	→	→	→	→	→	→	→	→	→
	073	NO	→	→	→	T	→	→	→	→	→	→	→	→	→	→	→	→	→
	074	NO	→	→	→	X	T	→	→	→	→	→	→	→	→	→	→	→	→
	081	NO	→	→	→	C	T	→	X	T	→	→	→	→	→	→	→	→	→
	091	NO	→	→	→	C	T	→	C	T	→	→	→	→	→	→	→	→	→
	111	NO	→	→	→	C	X	→	C	X	→	→	→	→	→	→	→	→	→
		AOT High Density Filter Assembly Compatibility																	
6011856	000					X	→	→	→	→	→	→	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used. (AOT-CCRD mounting compatibility is required. Reference ECP 422.)

ECP	DESCRIPTION
173	Reticle mount and objective lens assembly
197	Vacuum testing of AOT BREAK-IN 603
296	Connecting relay assembly BREAK-IN 602
301	Thermal instrumentation BREAK-IN 602 ONLY
318	Corrosion protection of exposed beryllium BREAK-IN 602
320	Blacken lens edges BREAK-IN 603
321	Incorporate eyepiece heaters BREAK-IN 603
353	Change pressure seal material BREAK-IN 603
360	Incorporate eyepiece locking lever BREAK-IN 603
410	Reposition eyepiece locking lever BREAK-IN 606 RETRO 605
421	Modify lens housing BREAK-IN 605 RETRO 604
422	CCRD mounting change BREAK-IN 606 RETRO 605
454	Improved pinning methods BREAK-IN 604
473	Incorporate shield to eliminate light scatter BREAK-IN 609 RETRO 605 through 608

ECP	DESCRIPTION
512	AOT high density filter assembly (sun filter) BREAK-IN 605
539	AOT reticle lamp change BREAK-IN 612 RETRO 604 through 611
540	AOT reticle knob change BREAK-IN 612 RETRO 604 through 611
542	AOT eyeguard plug BREAK-IN 612 RETRO 604 through 611
543	AOT counter moisture proofing and illumination BREAK-IN 612 RETRO 604 through 611
582	LTA-8 modifications AFFECTS 602 ONLY
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
633	AOT pressure seal protection and other flammability fixes BREAK-IN 612 RETRO 605 through 611
657	Conical sunshade and radar shield assembly for AOT BREAK-IN 618 RETRO 605 through 607, 609 through 617
697	AOT harness protective shield BREAK-IN 619 RETRO 605 through 607, 609 through 618
780	Taping of AOT cable assembly RETRO 605 through 618

Table 3-I. AOT Compatibility (Sheet 2 of 2)

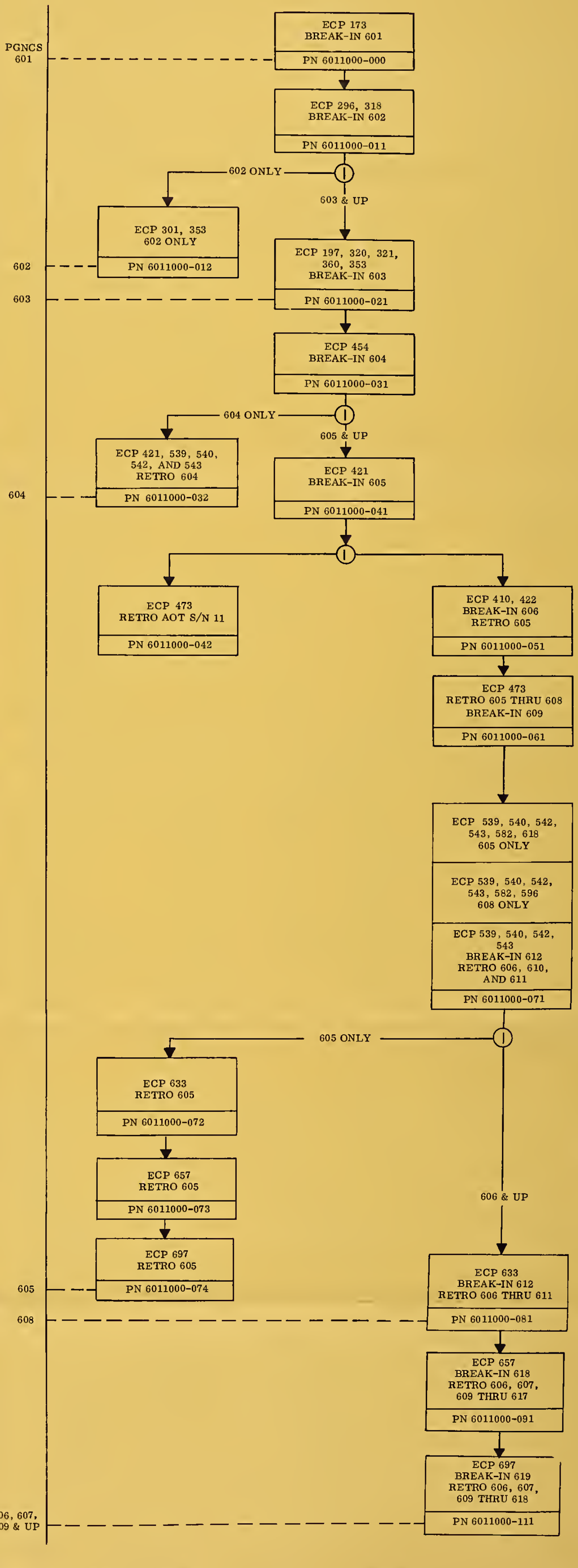
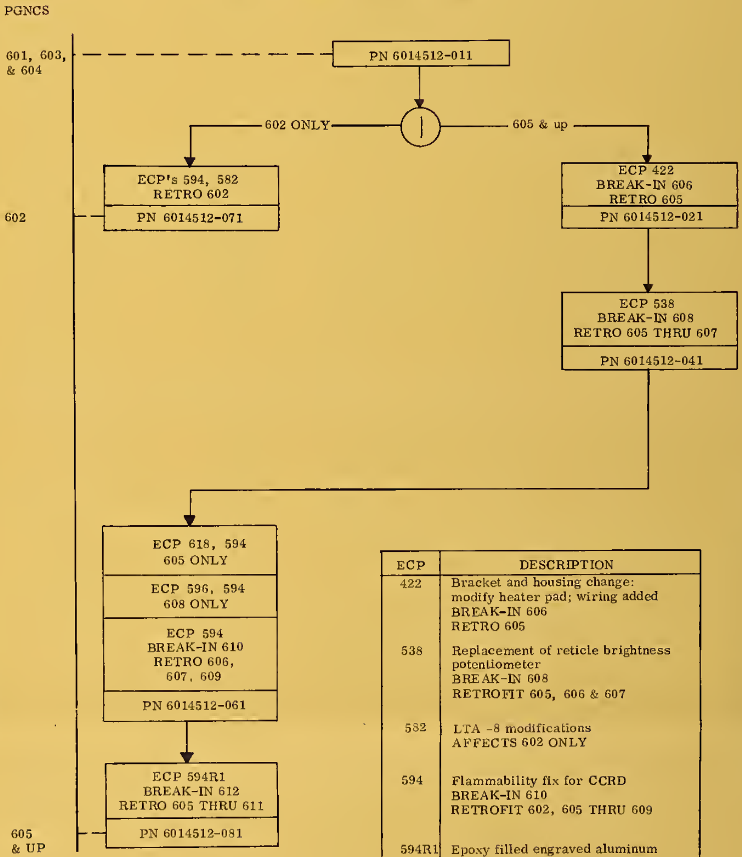


Table 3-IA. CCRD Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN 6015000 / SYSTEM SERIAL NUMBERS															
		011/601	021/602	031/603	041/604	051/605	061/606	071/607	081/608	091/609	101/610	111/611	121/612	131/613	141/614	151/615	161/616
6014512	011	X	T		X	NO	→	→	→	→	→	→	→	→	→	→	→
	021	NO	→		NO	T	→	→	→	→	→	→	→	→	→	→	→
	031	C	→		C	NO	→	→	→	→	→	→	→	→	→	→	→
	041	NO	→		NO	T	→	→	→	→	→	→	→	→	→	→	→
	051	C	→		C	NO	→	→	→	→	→	→	→	→	→	→	→
	061	NO	→		NO	T	→	→	→	→	→	→	→	→	→	→	→
	071	C	X		C	NO	→	→	→	→	→	→	→	→	→	→	→
	081	NO	→		NO	X	→	→	→	→	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used. (CCRD-AOT mounting compatibility is required. Reference ECP 422).

Table 3-IA. CCRD Compatibility (Sheet 2 of 2)



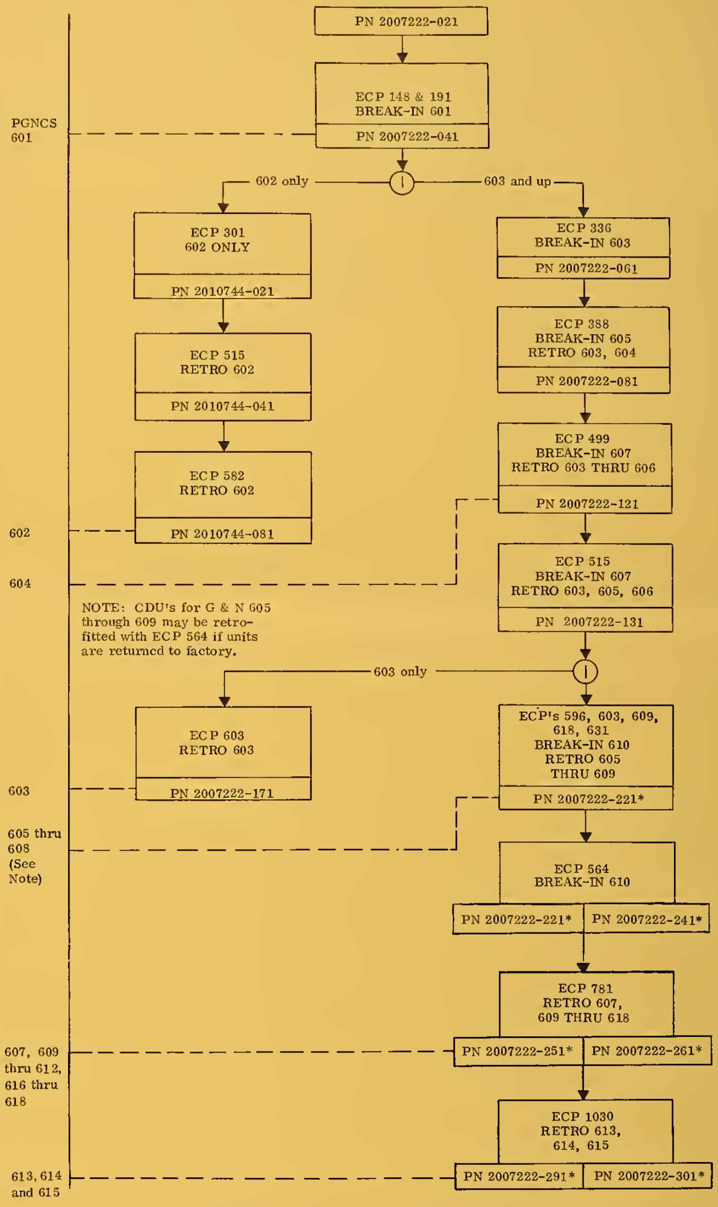
ECP	DESCRIPTION
422	Bracket and housing change: modify heater pad; wiring added BREAK-IN 606 RETRO 605
538	Replacement of reticle brightness potentiometer BREAK-IN 608 RETROFIT 605, 606 & 607
582	LTA -8 modifications AFFECTS 602 ONLY
594	Flammability fix for CCRD BREAK-IN 610 RETROFIT 602, 605 THRU 609
594R1	Epoxy filled engraved aluminum overlays BREAK-IN 612 RETROFIT 605 THRU 611
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY

Table 3-IB. CDU Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000										SYSTEM SERIAL NUMBERS							
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616	171 / 617	181 / 618
2007222	041	X	T	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	061	C	T	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	081	C	T	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	121	C	T	T	X	T	→	→	→	→	→	→	→	→	→	→	→	→	→
	131	C	T	→	C	T	→	→	→	→	→	→	→	→	→	→	→	→	→
	171	C	T	X	C	T	→	→	→	→	→	→	→	→	→	→	→	→	→
	221	C	T	C	C	X	→	→	→	→	→	→	→	→	→	→	→	→	→
	241	C	T	C	→	→	→	→	→	→	X*	→	→	→	→	→	→	→	→
	251	C	T	C	→	→	→	→	→	X	→	→	→	T	T	T	X	→	→
	261	C	T	C	→	→	→	→	→	X	→	→	→	T	T	T	X	→	→
	291	C	T	C	→	→	→	→	→	→	→	→	→	X	X	X	C	→	→
	301	C	T	C	→	→	→	→	→	→	→	→	→	X	X	X	C	→	→
2010744	021	C	T	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	041	C	T	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	081	C	X	T	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IB. CDU Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
148	Transformer change in CDU
191	CDU mode module change
301	Add thermal sensors 602 ONLY
336	Change potting material BREAK-IN 603
388	Corrosion and outgassing protection BREAK-IN 605 RETROFIT 603, 604
499	Addition of damper plate BREAK-IN 607 RETROFIT 603 THRU 606
515	Modify coarse system modules BREAK-IN 607 RETROFIT 602, 603, 605, 606
564*	Implementation of flat pack specifications ND 1002359A and ND 1002358B BREAK-IN 610
582	LTA-8 modifications AFFECTS 602 ONLY

*CDU's 2007222-241, 261, and 301 require modules 2007129-051, 2007140-041, and 2007141-041. If the above CDU's do not have all three modules, their P/N's are 2007222-221, 251, and 291, respectively. CDU's without ECP 564 are completely interchangeable with CDU's containing ECP 564.

ECP	DESCRIPTION
596	LM-2 modifications AFFECTS 608 ONLY
603	Capacitor replacement in CDU MSA and quadrature rejection module BREAK-IN 610 RETROFIT 603, 605 THRU 609
609	Elimination of CDU DAC saturation during coarse align mode BREAK-IN 610 RETROFIT 605 THRU 609
618	LM-3 modifications AFFECTS 605 ONLY
631	Replace RTV-102 with RTV-109 ECP 631 should be incorporated in PN 2007222-221. Incorporation of ECP 631 does not cause part number change. It may be included in lower part number assemblies.
781	CDU bolt change RETROFIT 609 THRU 618
1030	Replace 1010274 transformer in ECDU modules to increase reliability RETROFIT 613, 614, 615, and spares.

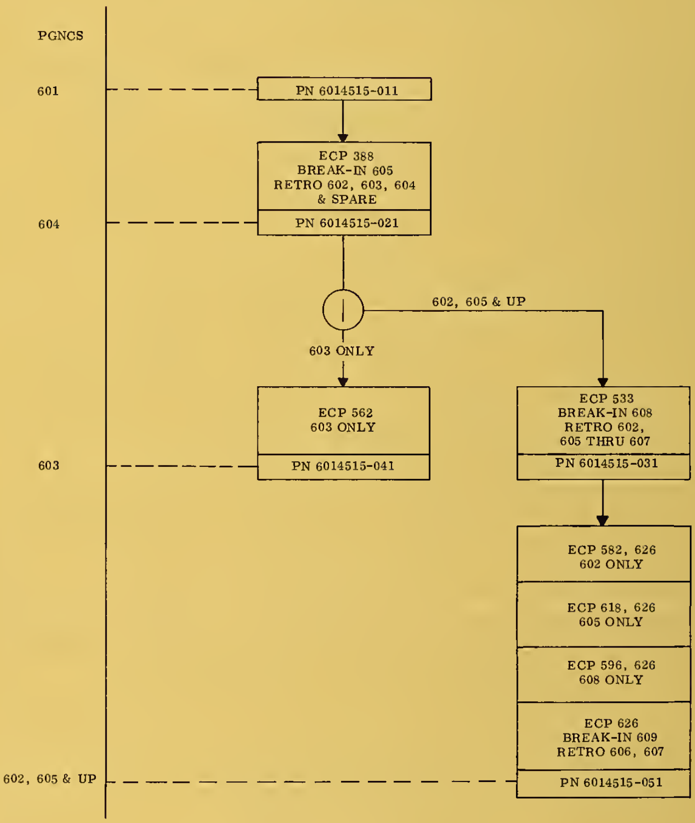
Table 3-IC. IMU and PTA Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000																	
		SYSTEM SERIAL NUMBERS																	
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616	171 / 617	181 / 618
6007001	011	X	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	021	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	031	X	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	041	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	051	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	061	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	071	C	T		X	T →	→	→	→	→	→	→	→	→	→	→	→	→	→
	081	C	T		C	T →	→	→	→	→	→	→	→	→	→	→	→	→	→
	091	C	T		C	T →	→	→	→	→	→	→	→	→	→	→	→	→	→
	101	C	T		C	X* →	→	→	→	→	→	T →	→	→	→	→	→	→	→
	111	C	T		C	T →	→	→	→	→	→	→	→	→	→	→	→	→	→
	121	C	T		C	X →	→	→	→	→	→	→	→	T	T	T	X →	→	→
	131	C	T		C	C →	→	→	→	→	→	→	→	X	X	X	C →	→	→
2010747	021	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	031	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	061	C	T		T →	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	081	C	X		X →	→	→	→	→	→	→	→	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

*See note 2 on sheet 2.

Table 3-ID. Interconnect Harness Group Compatibility (Sheet 2 of 2)



*NOTE: Retrofit of G & N 603 with ECP 626 is non-mandatory.

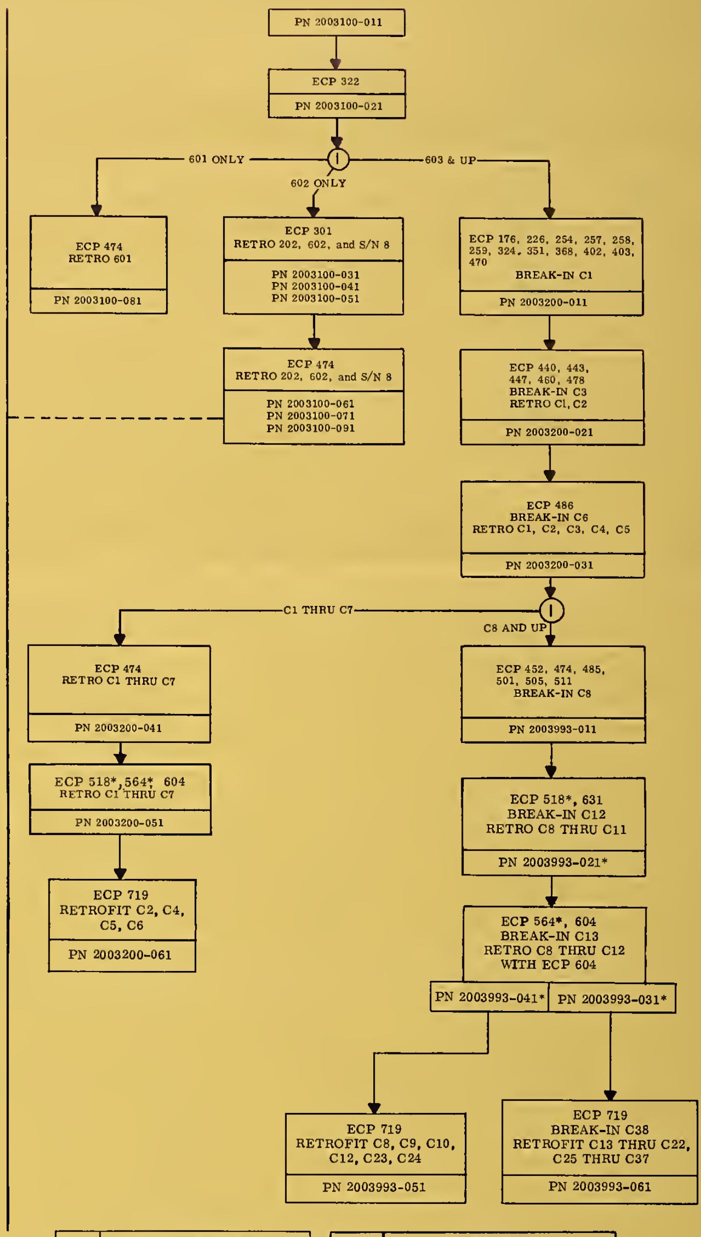
ECP	DESCRIPTION
388	Corrosion and outgassing protection BREAK-IN 605 RETROFIT 602, 603, 604 & SPARE
533	Incorporate uplink wires into harness "A" BREAK-IN 608 RETROFIT 602, 605 thru 607 & TWO SPARES
562	Replacement of LM-1 harness lacing tape G & N 603 ONLY
582	LTA-8 modifications AFFECTS 602 ONLY
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
626	Modification of LEM harness group for flammability protection BREAK-IN 609 RETROFIT 602, 603*, 605 THRU 608

Table 3-IE. LGC Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 SYSTEM SERIAL NUMBERS															
		011/601	021/602	031/603	041/604	051/605	061/606	071/607	081/608	091/609	101/610	111/611	121/612	131/613	141/614	151/615	161/616
2003100 2003100	011 thru 051	T	T		No →												
2003100	061	C	C		No →												
2003100	071	C	X		No →												
2003100	081	X	T		No →												
2003100	091	C	C		No →												
2003200	011	No →			No →												
2003200	021	No →			No →												
2003200	031	C	T		T →												
2003200	041	C	T		T →												
2003200	051	C	T		T →												
2003200	061	C	T		X →												
2003993	011	C	T		C	T	C	T →									
2003993	021	C	T		T →												
2003993	031	C	T		T →												
2003993	041	C	T		T →												
2003993	051	C	T		X →												
2003993	061	C	T		X →												

X	Required (Select one of above)
C	Compatible: as good or better than requirement. See ECP flow chart.
T	Not as good as requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-1E. LGC Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
176	Computer module vibration BREAK-IN C1
226	Aluminum to magnesium conversion of AGC trays BREAK-IN C1
254	Computer multilayer board layout (MLB) BREAK-IN C1
257	Redesign of rope & erasable drivers BREAK-IN C1
258	Redesign power supply module BREAK-IN C1
259	Redesign of erasable memory BREAK-IN C1
301	Thermal instrumentation 602 ONLY
322	Computer wiring changes BREAK-IN 601
324	Sense amplifier thresbold voltage stability change BREAK-IN C1
351	Alarm module temperature stabilization of warning integrator and improved oscillator fail alarm BREAK-IN C1
368	Improved power supply module relays BREAK-IN C1
402 '	Clear circuit driver modification BREAK-IN C1
403	Strobe adjustment BREAK-IN C1
440	"Clear rope" driver circuit modification BREAK-IN C3 RETROFIT C1 and C2
443	Replacement of short screws BREAK-IN C3 RETROFIT C1 and C2

*LGC Configuration for ECP 518 & 564

LGC	Logic Module	Power Supply	Tray A
2003200-051	2003121 or 2003888	2003892-011	2003092-041 -051 or -061
2003993-021 -041	2003121 or 2003888	2003892-011	2003092-041 or -061
2003993-031	2003888	2003892-011	2003092-041

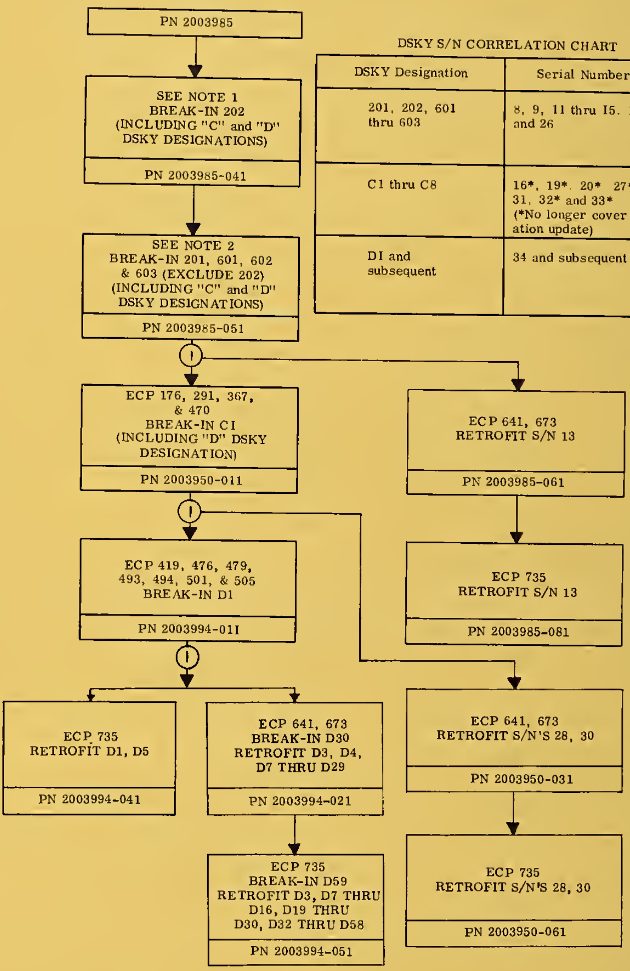
ECP	DESCRIPTION
447	Incorporation of plastic pads under tray A&B covers BREAK-IN C3 RETROFIT C1 and C2
452	Wiring change to accommodate auxiliary memory unit BREAK-IN C8
480	Addition of jumper wires in tray A BREAK-IN C3 RETROFIT C1 and C2
470	Random workmanship vibration BREAK-IN C1
474	Manufacture test connector jumpers to ground certain gate inputs BREAK-IN C8
478	Paint exposed surfaces on mid-tray spacer BREAK-IN C3 RETROFIT C1 and C2
485	Redesign power supply to remove 28 vdc regulator BREAK-IN C8
486	Cut pins on AGC power supply to remove 28 vdc regulator BREAK-IN C6 RETROFIT C1 thru C5
501	Implementation of flight processing spec BREAK-IN C8
505	Implementation of flight processing spec ND-1002341 and new diode
511	Correction of computer noise SCAFAL problem
518	Standby change on computer * BREAK-IN C12 RETROFIT C1 thru C11
564	Implementation of flat pack specifications ND 1002359A & ND 1002358B * BREAK-IN C13
604	Incorporation of E-memory vibration pads BREAK-IN C13 RETROFIT C1 THRU C12
631	Replace RTV-102 with RTV-109. ECP 631 should be incorporated in PN 2003993-031 and above. ECP 631 does not affect part number change. It may be included in other part number assemblies.
719	Alarm module modification, V-fail detection BREAK-IN C38 RETROFIT C2, C4, C5, C6, C8, C9, C10, C12, C23, C24, C13 thru C22, C25 thru C37

Table 3-IF. DSKY Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	061 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
2003985	021	T	→														
	031	T	→														
	041	T	→														
2003985	051	X	T		X	T	→	→	→	→	→	→	→	→	→	→	→
	061	C	T		C	T	→	→	→	→	→	→	→	→	→	→	→
	081	C	X		C	T	→	→	→	→	→	→	→	→	→	→	→
2003950 (SN 28, 30, 31 only)	011	C	→		C	T	→	→	→	→	→	→	→	→	→	→	→
	031	C	→		C	T	→	→	→	→	→	→	→	→	→	→	→
	061	C	→		C	T	→	→	→	→	→	→	→	→	→	→	→
2003994	011	C	→		C	T	→	→	→	→	→	→	→	→	→	→	→
	021	C	→		C	T	→	→	→	→	→	→	→	→	→	→	→
	041	C	→		C	T	→	→	→	→	→	→	→	→	→	→	→
	051	C	→		C	X	→	→	→	→	→	→	→	→	→	→	→

X	Required
C	Compatible: as good or better than requirement. See ECP flow chart.
T	Not as good as requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IF. DSKY Compatibility (Sheet 2 of 2)



DSKY S/N CORRELATION CHART

DSKY Designation	Serial Number (S/N)
201, 202, 601 thru 603	8, 9, 11 thru 15, 18, 25, and 26
C1 thru C8	16*, 19*, 20* 27*, 28, 30, 31, 32* and 33* (*No longer cover configuration update)
D1 and subsequent	34 and subsequent

NOTES:

1. Potted modules & housing change. No ECP number
2. Housing change. No ECP number

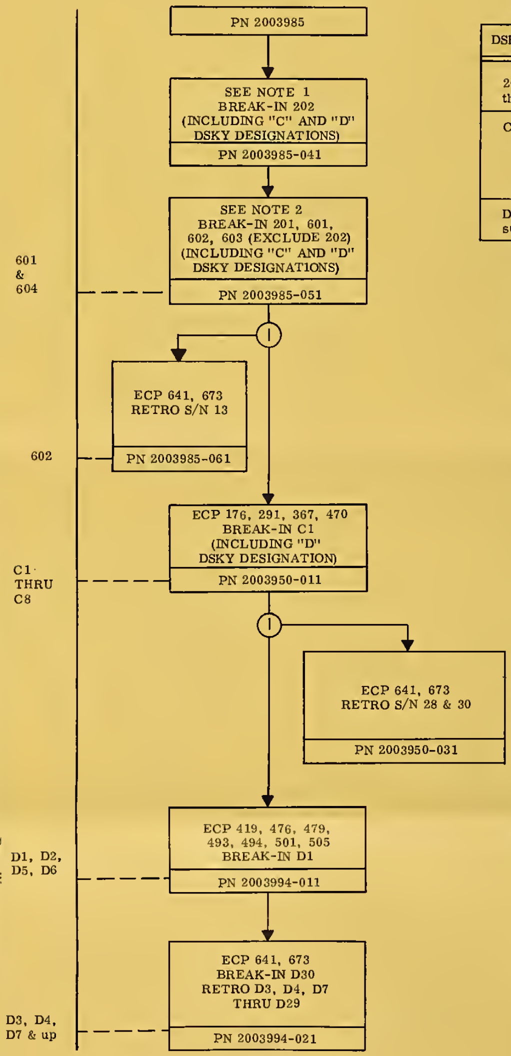
ECP	DESCRIPTION
176	DSKY module vibration BREAK-IN C1
291	DSKY alarm light redesign BREAK-IN C1
367	Addition of light duffusing paint to DSKY BREAK-IN C1
419	Indicator drive module relay replacement in DSKY BREAK-IN D1
470	Random workmanship vibration BREAK-IN C1
476	Painting of alarm indicator face BREAK-IN D1
479	DSKY teflon coated pushbutton shaft BREAK-IN D1
493	Y-line feedback base resistor BREAK-IN D1
494	DSKY wiring improvement BREAK-IN D1
501	Implementation of flight processing spec ND-1002313 BREAK-IN D1
505	Implementation of flight processing spec ND-1002314 and new diode BREAK-IN D1
641	Non-metallic materials modification for DSKY BREAK-IN D30 RETRO D3, D4, D7 thru D29, S/N's 13, 28, and 30
673	Redesign of DSKY pushbutton cap housing assembly leaf spring BREAK-IN D30 RETRO D3, D4, D7 thru D29, S/N's 13, 28, and 30
735	Addition of safety glass to cover DSKY EL and IL indicators BREAK-IN D59 RETROFIT D1, D3, D5, D7 thru D16, D19 thru D30, D32 thru D58, S/N's 13, 28, and 30

Table 3-IG. LGC Group Installation Kit Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6016000 / SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
6004000	000	X	→	→		NO	→	→	→	→	→	→	→	→	→	→	→
	011	NO	→	→		NO	→	→	→	→	→	→	→	→	→	→	→
	021	NO	→	→		T	→	→	NO	T	→	→	→	→	→	→	→
	031	NO	→	→		NO	→	→	X	NO	→	→	→	→	→	→	→
	041	NO	→	→		X	→	NO		NO	→	→	→	→	→	→	→
	051	NO	→	→		NO	→	X	NO	X	→	→	→	→	→	→	→

X Required per print
C Compatible: as good or better than print requirement. See ECP flow chart.
T Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO CANNOT be used.

Table 3-1F. DSKY Compatibility (Sheet 2 of 2)



DSKY S/N CORRELATION CHART

DSKY Designation	Serial Number (S/N)
201, 202, 601 thru 603	8, 9, 11 thru 15, 18, 25, and 26
C1 thru C8	16*, 19*, 20*, 27*, 28, 30, 31, 32*, 33* (*Configuration update no longer covered)
D1 and subsequent	34 and subsequent

ECP	DESCRIPTION
176	DSKY module vibration BREAK-IN C1
291	DSKY alarm light redesign BREAK-IN C1
367	Addition of light duffusing paint to DSKY BREAK-IN C1
419	Indicator drive module relay replacement in DSKY BREAK-IN D1
470	Random workmanship vibration BREAK-IN C1
476	Painting of alarm indicator face BREAK-IN D1
479	DSKY teflon coated pushbutton shaft BREAK-IN D1
493	Y-line feedback base resistor BREAK-IN D1
494	DSKY wiring improvement BREAK-IN D1
501	Implementation of flight processing spec ND-1002313 BREAK-IN D1
505	Implementation of flight processing spec ND-1002314 and new diode BREAK-IN D1
641	Non-metallic materials modification for DSKY BREAK-IN D30 RETRO D3, D4, D7 thru D29, S/N's 13, 28, and 30
673	Redesign of DSKY pushbutton cap housing assembly leaf spring BREAK-IN D30 RETRO D3, D4, D7 thru D29, S/N's 13, 28, and 30

NOTES:

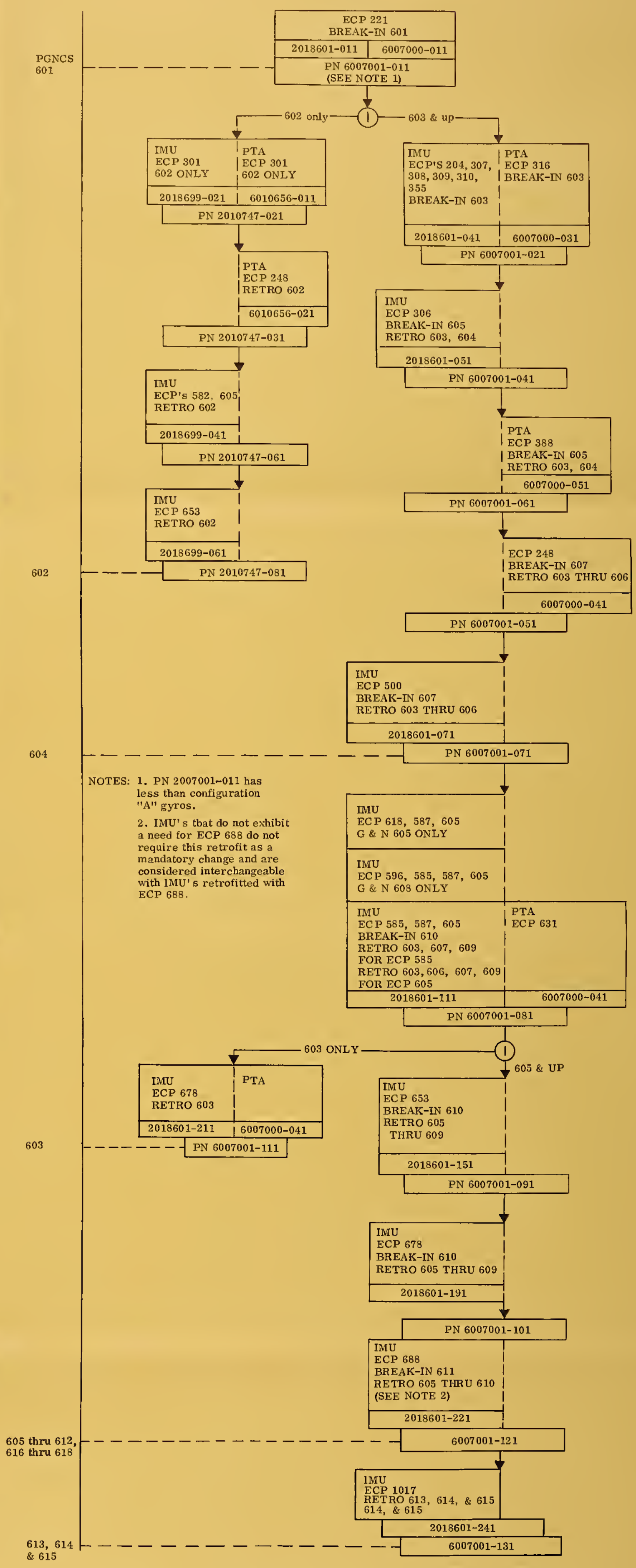
1. Potted modules and housing change. No ECP number.
2. Housing change. No ECP number.

Table 3-IG. LGC Group Installation Kit Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000								SYSTEM SERIAL NUMBERS							
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
6004000	000	X →	→	→		NO →	→	→	→	→	→	→	→	→	→	→	→
	011	NO →	→	→		NO →	→	→	→	→	→	→	→	→	→	→	→
	021	NO →	→	→		T →	→	→	NO	T →	→	→	→	→	→	→	→
	031	NO →	→	→		NO →	→	→	X	NO →	→	→	→	→	→	→	→
	041	NO →	→	→		X →	→	→	NO	X →	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IC. IMU and PTA Compatibility (Sheet 2 of 2)



NOTES: 1. PN 2007001-011 has less than configuration "A" gyros.

2. IMU's that do not exhibit a need for ECP 688 do not require this retrofit as a mandatory change and are considered interchangeable with IMU's retrofitted with ECP 688.

ECP	DESCRIPTION
204	Thermal control circuitry change. BREAK-IN 603
221	Z axis IRIG rotation BREAK-IN 601
248	Pulse torque power supply change. BREAK-IN 607 RETROFIT 602 thru 606
301	Thermocouple addition 602 ONLY
306	Mount harness "B" cable clamp on IMU BREAK-IN 605 RETRO 603, 604
307	Middle axis assembly clamp changes BREAK-IN 603
308	Stable member heat transfer change BREAK-IN 603
309	PIP Temperature reduction and temperature alarm test BREAK-IN 603
310	IMU cross coupling change BREAK-IN 603
316	Potting voids BREAK-IN 603
355	IRIG change BREAK-IN 603
388	Corrosion and outgassing protection BREAK-IN 605 RETROFIT 603, 604
500	PIP preamplifier change BREAK-IN 607 RETROFIT 603 thru 606

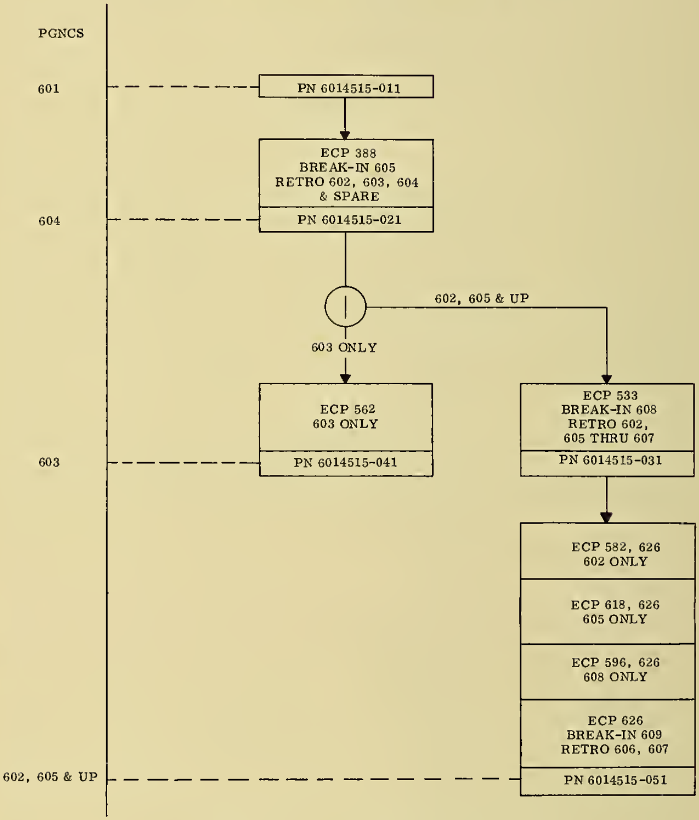
ECP	DESCRIPTION
582	LTA-8 modifications AFFECTS 602 ONLY
585	PIP preamplifier capacitor replacement BREAK-IN 610 RETROFIT 603, 607, and 609
587	IRIG gyro end cap replacement. ECP 587 should be incorporated in PN 6007001-081 and higher. Incorporation of ECP 587 does not cause part number changes. It may be included in lower part number assemblies.
596	LM-2 modifications AFFECTS 608 ONLY
605	IMU blanket removal BREAK-IN 610 RETROFIT 602, 603, 605 thru 607
618	LM-3 modifications AFFECTS 605 ONLY
631	Replace RTV-102 with RTV-109 ECP 631 should be incorporated in PN 6007001-081 and higher. Incorporation of ECP 631 does not cause part number changes. It may be included in lower part number assemblies.
653	Modification of IMU wiring to reduce IRIG pre-amp oscillation BREAK-IN 610 RETROFIT 602, 605 thru 609
678	IRIG end cap change BREAK-IN 610 RETROFIT 603, 605 thru 609
688	Modification of IMU to reduce sporadic oscillation of IRIG preamp BREAK-IN 611 RETROFIT 605 thru 610 (See note 2.)
1017 & 1032	Replace blower motor in IMU to increase reliability. RETROFIT 613, 614, 615, and spares.

Table 3-ID. Interconnect Harness Group Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS																	
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616	171 / 617	181 / 618
6014515	011	X	T →																→
	021	C	T →	→	X	T →													→
	031	C	T →	→	C	T →													→
	041	C	T	X	C	T →													→
	051	C	X	C →	→	X →													→

X Required per print
C Compatible: as good or better than print requirement. See ECP flow chart.
T Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO CANNOT be used.

Table 3-ID. Interconnect Harness Group Compatibility (Sheet 2 of 2)



*NOTE: Retrofit of G & N 603 with ECP 626 is non-mandatory.

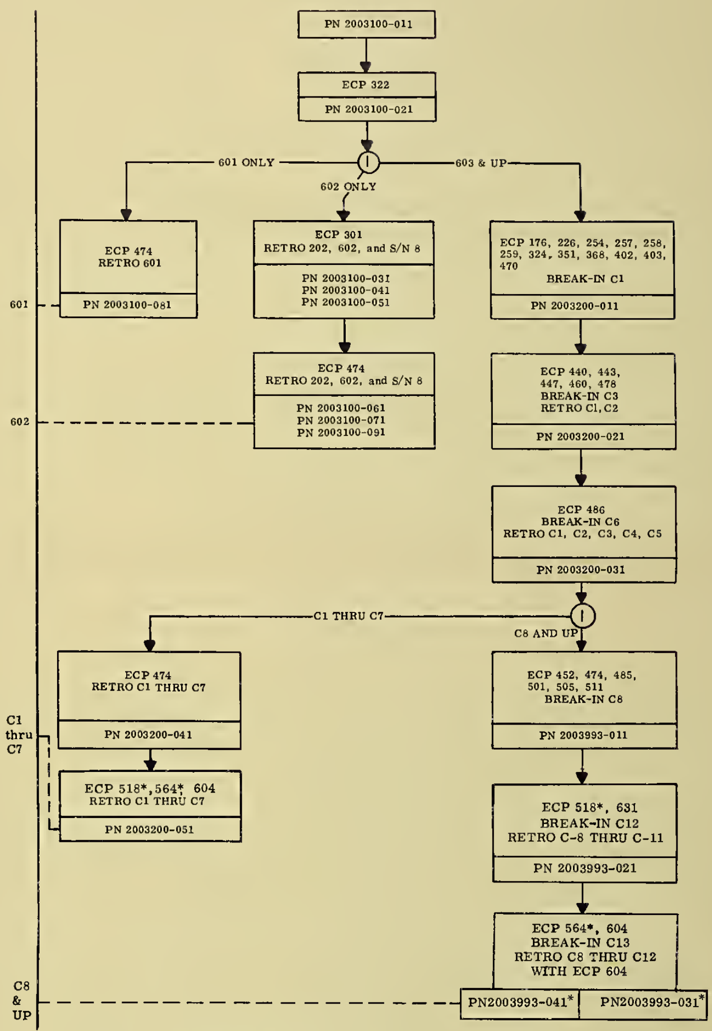
ECP	DESCRIPTION
388	Corrosion and outgassing protection BREAK-IN 605 RETROFIT 602, 603, 604 & SPARE
533	Incorporate uplink wires into harness "A" BREAK-IN 608 RETROFIT 602, 605 thru 607 & TWO SPARES
562	Replacement of LM-1 harness lacing tape G & N 603 ONLY
582	LTA-8 modifications AFFECTS 602 ONLY
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
626	Modification of LEM harness group for flammability protection BREAK-IN 609 RETROFIT 602, 603*, 605 THRU 608

Table 3-IE. LGC Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
2003100	011	T	T		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	021	T	T		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	031	T	T		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	041	T	T		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	051	T	T		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	061	C	C		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	071	C	X		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	081	X	T		No	—	—	—	—	—	—	—	—	—	—	—	→
2003100	091	C	C		No	—	—	—	—	—	—	—	—	—	—	—	→
2003200	011	No	→		No	—	—	—	—	—	—	—	—	—	—	—	→
2003200	021	No	→		No	—	—	—	—	—	—	—	—	—	—	—	→
2003200	031	C	T		T	—	—	—	—	—	—	—	—	—	—	—	→
2003200	041	C	T		T	—	—	—	—	—	—	—	—	—	—	—	→
2003993	051	C	T		X	—	—	—	—	—	—	—	—	—	—	—	→
2003993	011	C	T		C	T	C	T	—	—	—	—	—	—	—	—	→
2003993	021	C	T		T	—	—	—	—	—	—	—	—	—	—	—	→
2003993	031	C	T		X	—	—	—	—	—	—	—	—	—	—	—	→
2003993	041	C	T		X	—	—	—	—	—	—	—	—	—	—	—	→

X	Required (Select one of above)
C	Compatible: as good or better than requirement. See ECP flow chart.
T	Not as good as requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IE. LGC Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
176	Computer module vibration BREAK-IN C1
226	Aluminum to magnesium conversion of AGC trays BREAK-IN C1
254	Computer multilayer board layout (MLB) BREAK-IN C1
257	Redesign of rope & erasable drivers BREAK-IN C1
258	Redesign power supply module BREAK-IN C1
259	Redesign of erasable memory BREAK-IN C1
301	Thermal instrumentation 602 ONLY
322	Computer wiring changes BREAK-IN 601
324	Sense amplifier threshold voltage stability change BREAK-IN C1
351	Alarm module temperature stabilization of warning integrator and improved oscillator fail alarm BREAK-IN C1
368	Improved power supply module relays BREAK-IN C1
402	Clear circuit driver modification BREAK-IN C1
403	Strobe adjustment BREAK-IN C1
440	"Clear rope" driver circuit modification BREAK-IN C3 RETROFIT C1 and C2
443	Replacement of short screws BREAK-IN C3 RETROFIT C1 and C2

ECP	DESCRIPTION
447	Incorporation of plastic pads under tray A&B covers BREAK-IN C3 RETROFIT C1 and C2
452	Wiring change to accommodate auxiliary memory unit BREAK-IN C8
460	Addition of jumper wires in tray A BREAK-IN C3 RETROFIT C1 and C2
470	Random workmanship vibration BREAK-IN C1
474	Manufacture test connector jumpers to ground certain gate inputs BREAK-IN C8
478	Paint exposed surfaces on mid-tray spacer BREAK-IN C3 RETROFIT C1 and C2
485	Redesign power supply to remove 28 vdc regulator BREAK-IN C8
486	Cut pins on AGC power supply to remove 28 vdc regulator BREAK-IN C8 RETROFIT C1 thru C5
501	Implementation of flight processing spec BREAK-IN C8
505	Implementation of flight processing spec ND-1002341 and new diode
511	Correction of computer noise SCAFAL problem
518	Standby change on computer* BREAK-IN C12 RETROFIT C1 thru C11
564	Implementation of flat pack specifications ND 1002359A & ND 1002358B * BREAK-IN C13
604	Incorporation of E-memory vibration pads BREAK-IN C13 RETROFIT C1 THRU C12
631	Replace RTV-102 with RTV-109. ECP 631 should be incorporated in PN 2003993-031 and above. ECP 631 does not affect part number change. It may be included in other part number assemblies.

*LGC Configuration for ECP 518 & 564

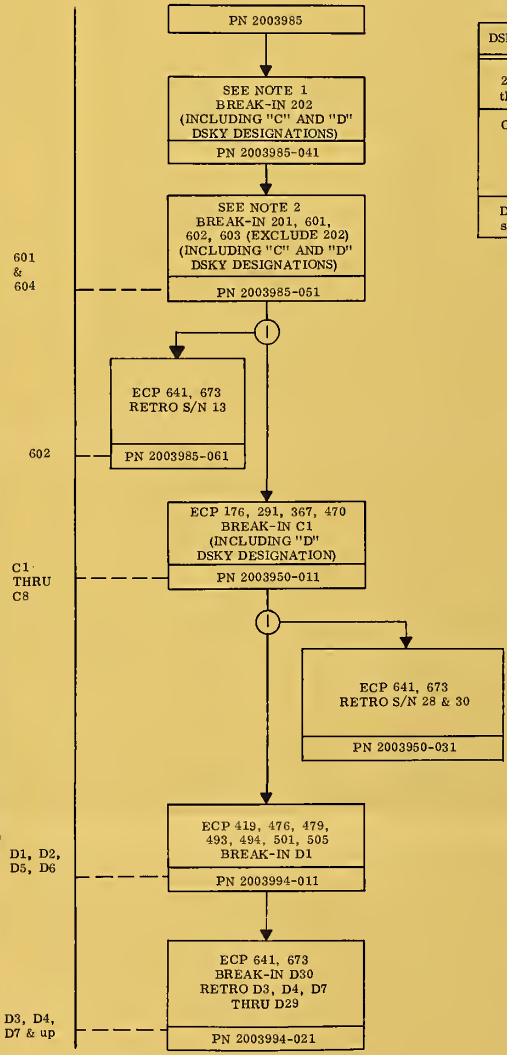
LGC	Logic Module	Power Supply	Tray A
2003200-051	2003121 or 2003888	2003892-011	2003092-041 -051 or -061
2003993-021 -041	2003121 or 2003888	2003892-011	2003092-041 or -061
2003993-031	2003888	2003892-011	2003092-041

Table 3-IF. DSKY Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
2003985	021	T	→														
	031	T	→														
	041	T	→														
2003985	051	X	T →	→	X	T	→	→	→	→	→	→	→	→	→	→	→
	061	C	X	T	C	T	→	→	→	→	→	→	→	→	→	→	→
2003950 (SN 28, 30, 31 only)	011	C	→	T	C	T	→	→	→	→	→	→	→	→	→	→	→
	031	C	→	T	C	T	→	→	→	→	→	→	→	→	→	→	→
2003994	011	C	→	T	C	T	→	→	→	→	→	→	→	→	→	→	→
	021	C	→	X	C	X	→	→	→	→	→	→	→	→	→	→	→

X	Required
C	Compatible: as good or better than requirement. See ECP flow chart.
T	Not as good as requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IF. DSKY Compatibility (Sheet 2 of 2)



DSKY S/N CORRELATION CHART

DSKY Designation	Serial Number (S/N)
201, 202, 601 thru 603	8, 9, 11 thru 15, 18, 25, and 26
C1 thru C8	16*, 19*, 20*, 27*, 28, 30, 31, 32*, 33* (*Configuration update no longer covered)
D1 and subsequent	34 and subsequent

ECP	DESCRIPTION
176	DSKY module vibration BREAK-IN C1
291	DSKY alarm light redesign BREAK-IN C1
367	Addition of light duffusing paint to DSKY BREAK-IN C1
419	Indicator drive module relay replacement in DSKY BREAK-IN D1
470	Random workmanship vibration BREAK-IN C1
476	Painting of alarm indicator face BREAK-IN D1
479	DSKY teflon coated pushbutton shaft BREAK-IN D1
493	Y-line feedback base resistor BREAK-IN D1
494	DSKY wiring improvement BREAK-IN D1
501	Implementation of flight processing spec ND-1002313 BREAK-IN D1
505	Implementation of flight processing spec ND-1002314 and new diode BREAK-IN D1
641	Non-metallic materials modification for DSKY BREAK-IN D30 RETRO D3, D4, D7 thru D29, S/N's 13, 28, and 30
673	Redesign of DSKY pushbutton cap housing assembly leaf spring BREAK-IN D30 RETRO D3, D4, D7 thru D29, S/N's 13, 28, and 30

NOTES:

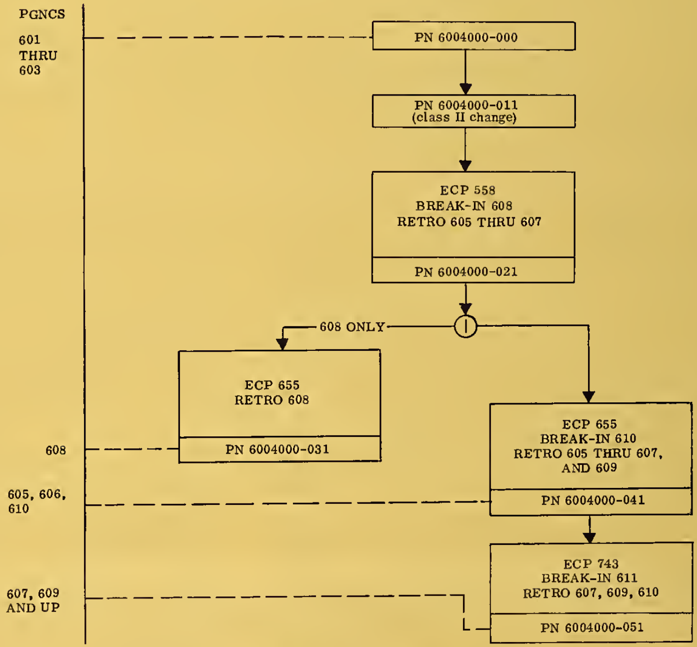
1. Potted modules and housing change. No ECP number.
2. Housing change. No ECP number.

Table 3-IG. LGC Group Installation Kit Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6016000															
											SYSTEM SERIAL NUMBERS						
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
6004000	000	X	→	→		NO	→	→	→	→	→	→	→	→	→	→	→
	011	NO	→	→		NO	→	→	→	→	→	→	→	→	→	→	→
	021	NO	→	→		T	→	→	NO	T	→	→	→	→	→	→	→
	031	NO	→	→		NO	→	→	X	NO	→	→	→	→	→	→	→
	041	NO	→	→		X	→	→	NO	X	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IG. LGC Group Installation Kit Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
558	Replacement of LGC/LM mounting bolts and brackets BREAK-IN 608 RETROFIT 605 THRU 607
655	New LGC mounting bolts and spacers BREAK-IN 610 RETROFIT 605 THRU 609
743	New configuration of installation kit BREAK-IN 611 RETROFIT 607, 609, 610

Table 3-IH. Jumper Module (Aurora - PN 2021101) Compatibility

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
2003076	011	T*	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	021	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
	031	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→

* Can be used in slots B4, B5, and B6 of "pre C" computers or in slot B4 of "C" computers.

CAUTION: Do not use 2003076-011 module in slots B5 and B6 of "C" computers. Use of 2003076-011 modules in these slots can damage the "C" computers.

X	Required
C	Compatible: as good or better than requirement.
T	Not as good as requirement, but can be used for testing.
NO	CANNOT be used.

Table 3-IJ. Rope Module (Aurora Program Assembly) Compatibility

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6018000															
		SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
2021101	011	T															→
	021	X															→
	031	X															→

X	Required
C	Compatible: as good or better than requirement.
T	Not as good as requirement, but can be used for testing:
NO	CANNOT be used.

Aurora Program Assembly Part Number	Module Part Number and Location					
	Module B1	Module B2	Module B3	Module B4 (See Note 1)	Module B5 (See Notes 1 and 2)	Module B6 (See Notes 1 and 2)
2021101-011 (Aurora 85)	2003053-061	2003053-071	2003053-081	2003076-021	2003076-021	2003076-021
2021101-021 (Aurora 88) (See Note 3)	2003053-061 or 2003972-011	2003053-171 or 2003972-091	2003053-181 or 2003972-111	2003076-021	2003076-021	2003076-021
2021101-031 (Aurora 88)	2003972-011	2003972-091	2003972-111	2003076-021	2003076-021	2003076-021

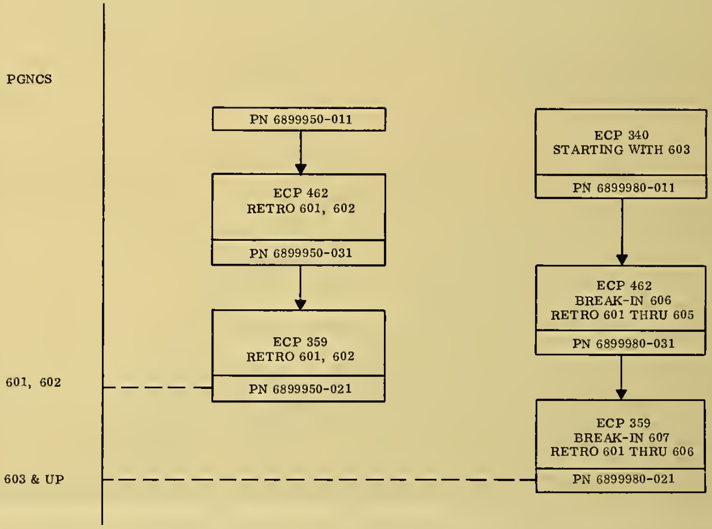
NOTES:
1. Refer to table 3-IH for jumper module compatibility.
2. Use of modules in slots B5 and B6 is optional.
3. When 2021101-021 assembly contains all 2003972 configuration modules in slots B1, B2, and B3, the set shall be identified as 2021101-031.

Table 3-IK. Nav Base Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000															
		SYSTEM SERIAL NUMBERS															
		011/601	021/602	031/603	041/604	051/605	061/606	071/607	081/608	091/609	101/610	111/611	121/612	131/613	141/614	151/615	161/616
6899950	011	T	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
6899950	021	X	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
6899950	031	T	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
6899980	011	C	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→
6899980	021	C	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→
6899980	031	C	→	NO	→	→	→	→	→	→	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IK. Nav Base Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
340	Nav base redesign STARTING WITH 603
359	Replacement of IMU mounting bolts BREAK-IN 607 RETRO 601 thru 606
462	Addition of ground strap to LM nav base BREAK-IN 606 RETRO 601 thru 605

Table 3-IL. PSA Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS																	
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616	171 / 617	181 / 618
6007200	011	X	T		T →														
	021	C	T		T →														
	031	C	T		T →														
	041	C	T		T →														
	051	C	T		X	T →													
	071	C	T		C	T →													
	081	C	T		C	X →													
6010655	011	T →			T →														
	021	T →			T →														
	031	T	X		T →														

X	Required per print
C	Compatible: as good as or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-IJ. Signal Conditioner Assembly Compatibility (Sheet 2 of 2)

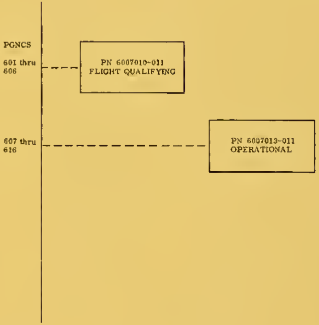
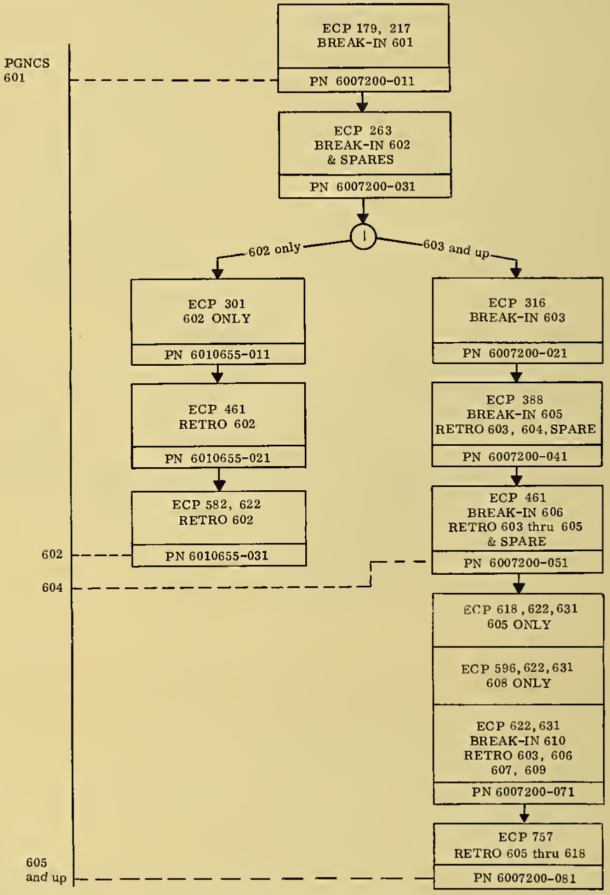


Table 3-IL. PSA Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
179	G and N filter change BREAK-IN 601
217	Delete signal conditioner power supply assembly BREAK-IN 601
263	New helicoil and screw BREAK-IN 602 and spare
301	Thermal instrumentation BREAK-IN 602
316	Potting voids in header BREAK-IN 603
388	Corrosion and outgassing protection BREAK-IN 605 RETROFIT 603, 604, spare 1
461	Change gimbal servo amplifier BREAK-IN 606 RETROFIT 602 thru 605
582	LTA-8 modifications AFFECTS 602 ONLY

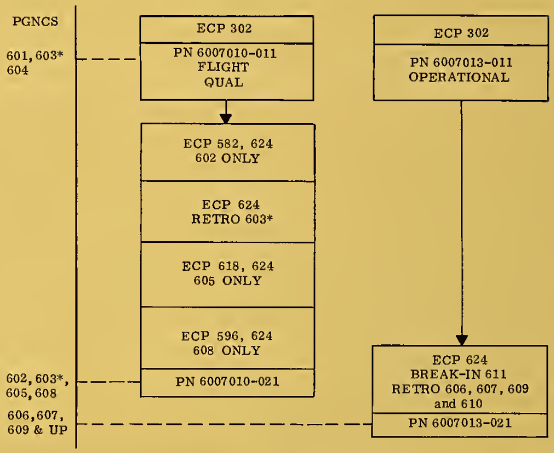
ECP	DESCRIPTION
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
622	Non-metallic materials flammability modification for PSA BREAK-IN 610 RETROFIT 602, 603, 605 and up
631	Replace RTV-102 with RTV-109. ECP 631 should be incorporated in PN 6007200-071 and above. ECP 631 does not affect part number change. It may be included in other part number assemblies.
757	Design changes to correct LEM PSA reverse power problem RETROFIT 605 thru 618

Table 3-1M. Signal Conditioner Assembly Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS															
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
6007010	011	X	T	X*	X	T	NO →	→	T	NO →	→	→	→	→	→	→	→
	021	C	X →	→	C	X	NO →	→	X	NO →	→	→	→	→	→	→	→
6007013	011	NO →	→	→	→	→	T →	→	NO	T →	→	→	→	→	→	→	→
	021	NO →	→	→	→	→	X →	→	NO	X →	→	→	→	→	→	→	→

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement. but can be used for testing. See ECP flow chart.
NO	CANNOT be used.
*	See note on sheet 2 of 2.

Table 3-IM. Signal Conditioner Assembly Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
302	Manufacture of Block II and LM signal conditioner assemblies BREAK-IN 601
582	LTA-8 modifications AFFECTS 602 ONLY
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
624	Non-metallic materials flammability modification for SCA BREAK-IN 611 RETRO 602, 603*, 605 THRU 610

*NOTE: Retrofit of G & N 603 with ECP 624 is non-mandatory.

Table 3-IN. Signal Conditioner Assembly Installation Kit Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000											SYSTEM SERIAL NUMBERS				
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616
6007021		X	→	→	→	→	NO	→	X	NO	→	→	→	→	→	→	→
6007020		NO	→	→	→	→	X	→	NO	X	→	→	→	→	→	→	→

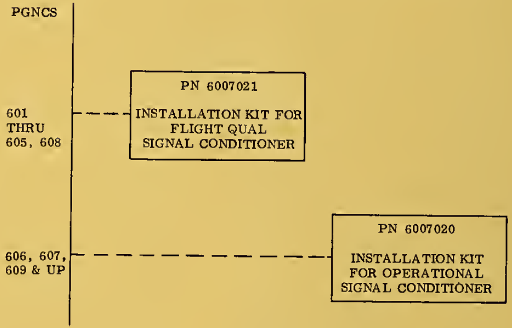
X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.

Table 3-I. LEM PGNCS Components

Component	Part Number	Location
Nav base	6899950 6899980	Attached to LEM structure in unpressurized compartment above astronauts' heads by means of nav base support.
PSA	6007200 6010655	Mounted on coldplate on lower section of after crew compartment wall below CDU.
Signal conditioner assembly (SCA)		Attached to top of PSA.
Flight qualification	6007010-011	
Operational	6007013-011	

(Sheet 3 of 3)

Table 3-IN. Signal Conditioner Assembly Installation Kit Compatibility (Sheet 2 of 2)



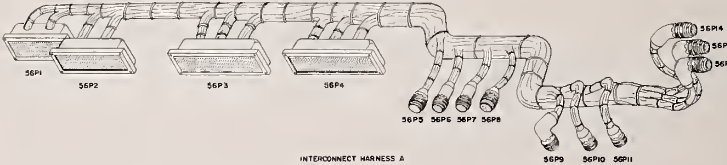
3-2 PGNCS INTERCONNECT HARNESS GROUP (LEM)

The PGNCS interconnect harness group (composed of interconnect harnesses A and B) interconnects the components of the PGNCS and provides the electrical interface between the PGNCS and other LEM systems. The IMU and PTA are interconnected by harness B. Harness A interconnects the PSA, CDU, LGC, and signal conditioner. The two harnesses are connected to each other by vehicle cables. Table 3-II lists the harness connectors and the components or cable to which they are mated. Figure 3-1A illustrates the PGNCS interconnect harness group.

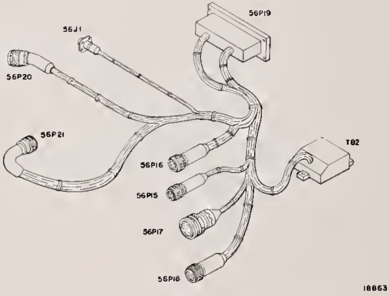
Table 3-II. PGNCS Harness Interconnections

PGNCS Harness Connector	Component	Component Connector
	Harness A	
56P1	Signal conditioner	30J1
56P2	PSA	45J19
56P3	CDU	40J53
56P4	LGC	05A1J1*
56P5	LEM spacecraft harness	J221
56P6	LEM spacecraft harness	J220
56P7	LEM spacecraft harness	J219
56P8	LEM spacecraft harness	J222
56P9	LEM spacecraft harness	J218
56P10	LEM spacecraft harness	J217
56P11	LEM spacecraft harness	J223
56P12	LEM spacecraft harness	J224
56P13	LEM spacecraft harness	J215
56P14	LEM spacecraft harness	J216
	Harness B	
56P15	LEM spacecraft harness	J226
56P16	LEM spacecraft harness	J227
56P17	LEM spacecraft harness	J228
56P18	LEM spacecraft harness	J225
56P19	PTA	35A2J19
56P20	IMU	35A1J2
56P21	IMU	35A1J1
56J1	LEM spacecraft harness	P230

* May be designated A51



INTERCONNECT HARNESS A



INTERCONNECT HARNESS B

Figure 3-1A. PGNCS Interconnect Harness Group

3-3 NAVIGATION BASE ASSEMBLY

The navigation base assembly (nav base), figure 3-2 and 3-2A, is a lightweight mount which supports, in critical alignment, the IMU and AOT. The nav base, constructed of one inch diameter, aluminum alloy tubing, weighs approximately three pounds. It consists of a center ring supporting four legs which extend from either side. The ring is approximately 14 inches in diameter and each of the four legs is approximately ten inches long. The IMU is mounted to the ends of the four legs on one side of the ring. The AOT and the abort sensor assembly are mounted to the opposite ends of the legs. The nav base is bolted to the LEM structure above the astronauts' head by three mounting pads on the center ring. An electrical grounding strap is attached to the center ring and to the LEM structure when the nav base is installed in the LEM.

3-4 INERTIAL MEASURING UNIT

The IMU (figure 3-3) is a three gimbal system designed for movement of the LEM about ali axes of the gyro-stabilized inner gimbal (stable member). To provide lightweight, rigid construction, the stable member is machined from a beryllium block and the gimbals are constructed of an aluminum alloy. The weight of the IMU is approximately 42 pounds, and the gimbal case is approximately 12.5 inches in diameter.

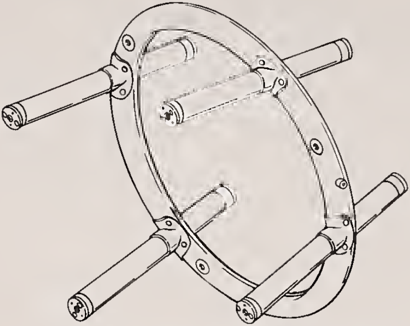


Figure 3-2. Navigation Base Assembly, P/N 6899950

Three Apollo II IRIG's hold the stable member in a stabilized condition. Accelerations along any component of any of the three orthogonal axes of the stable member are sensed by one or more of the three 16 PIP accelerometers. Intergimbal assemblies physically support the gimbals and pass electrical signals between them. The temperature of the IMU is maintained at the desired level by a system of heaters, blowers, and coolant passages. The IMU is pressurized to aid in convection cooling.

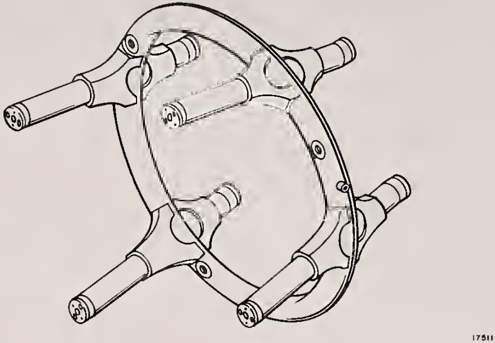


Figure 3-2A. Navigation Base Assembly, P/N 6899980

3-4.1 STABLE MEMBER. The stable member, or inner gimbal, is suspended by two intergimbal assemblies inside the middle gimbal. It is free to rotate without restriction about the inner gimbal (IG) axis. Holes are machined in the beryllium block to receive the three Apollo II IRIG's and three 16 PIP's. Accelerometer preamplifiers, stable member heaters, temperature control circuitry and thermostats, a ducosyn transformer, and two safety thermostats are all attached to the stable member.

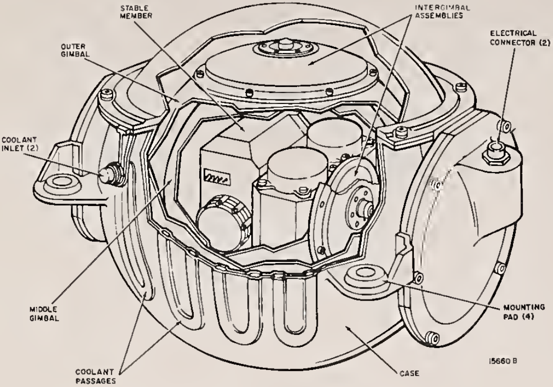


Figure 3-3. Inertial Measuring Unit

3-4.1.1 Gyroscopes. The three gyroscopes (gyros) on the stable member are Apollo II IRIG types. Figure 3-4 shows the location of the gyros on the stable member.

Ducosyns are used for magnetic suspension of the gyro rotor and for signal and torque generation. The signal generator ducosyn is located at one end of the float; the torque generator ducosyn is located at the other end.

The gyro wheel assembly operates as a hysteresis synchronous motor. The hub of the wheel is made of beryllium and the rim is made of heavy steel. This method of construction concentrates the weight at the rim, giving the wheel a high inertial moment.

3-4.1.2 Accelerometers. The LEM IMU uses three 16 PIP devices for sensing acceleration. Figure 3-4 shows the orthogonal placement of the 16 PIP's on the stable member. The 16 PIP is basically a cylindrical float with a pendulous mass unbalance and is pivoted with respect to a case. Ducosyns are located at each end of the float for magnetic suspension and signal and torque generation.

3-4.1.3 Stable Member Mounted Electronics. Table 3-III gives the locations and functions of electronics modules which are mounted in the IMU.

3-4.2 MIDDLE GIMBAL. The middle gimbal is suspended by two intergimbal assemblies inside the outer gimbal. It, in turn, supports the stable member. Slip ring assemblies in the intergimbal assemblies provide a means of carrying electrical signals between the outer gimbal and the stable member.

3-4.3 OUTER GIMBAL. The outer gimbal is similar in configuration to the middle gimbal, being suspended inside the supporting gimbal, or case, by two intergimbal assemblies. The outer gimbal has two thermostatically controlled axial-flow blowers mounted in its walls to force air from the vicinity of the middle gimbal to the walls of the case, where heat is carried away by a coolant solution circulating through passages in the case.

3-4.4 SUPPORTING GIMBAL. The supporting gimbal (case) is a spherical enclosure which supports the three gimbals described in the preceding paragraphs. The outer gimbal is suspended inside the case by two intergimbal assemblies which allow complete freedom of rotation. The walls of the case contain coolant passages through which a water-glycol solution is circulated to dissipate heat generated by inertial components and electronic modules. Two quick-disconnect fittings connect the coolant passages to the LEM coolant supply. The case is surrounded by insulating material to prevent condensation of moisture on the coolant passages.

Electrical interface between the IMU and the remainder of the PGNCS is accomplished by two electrical connectors on the case. A precision resolver alignment assembly module and a blower control relay are mounted on the resolver inter-gimbal assembly of the outer gimbal. Their functions are described in table 3-III. The resolver alignment assembly is accessible from outside the case.

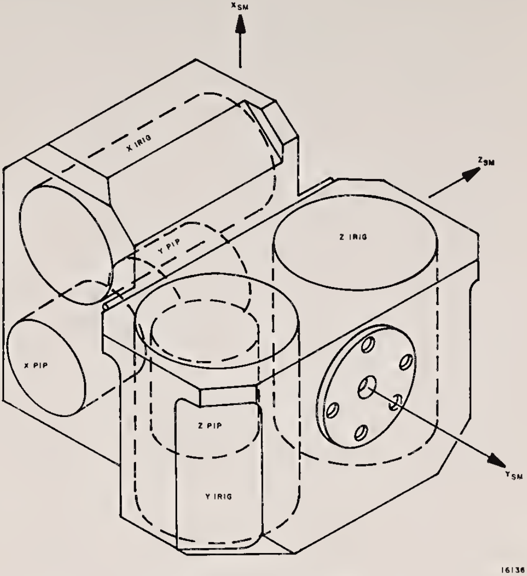


Figure 3-4. IMU Stable Member

Table 3-III. Locations and Functions of IMU Electronics

Module or Component	Part Number	Location and Function
Blower control module assembly	2007171 (system 601 and 602) 2007172 (system 603)	Stable member (SM): Removes power from blower control relay in response to request from blower control thermostat.
Blower control thermostat and heater assembly	2018635 (system 601 and 602) 2018825 (system 603)	SM: Controls on-off action of blower motors on outer gimbal.
Temperature control module assembly	2007064	SM: Applies power to gyro, accelerometer, and stable member heaters in response to request from temperature control thermostat.
Temperature control thermostat and heater assembly	2018637	SM: Controls operation of temperature control module to maintain proper heat in inertial components.
Stable member heater assembly (2)	2018641	SM: Supplement heat generated by inertial component heaters.
Safety thermostat (2)	1001485	SM: Disable all IMU heaters in the event of an extreme overheat condition.
Temperature alarm module assembly	2007170	SM: Signals LGC that an overheat or underheat condition is present.
Temperature alarm thermostat assembly	2018636 (system 601 and 602)	SM: Controls operation of temperature alarm module assembly.
Temperature alarm thermostat and heater assembly (high)	2018823 (system 603)	SM: Controls high temperature overheat condition and operation of temperature alarm module.
Temperature alarm thermostat and heater assembly (low)	2018824 (system 603)	SM: Controls low temperature under heat condition and operation of temperature alarm module.

(Sheet 1 of 2)

Table 3-III. Locations and Functions of IMU Electronics

Module or Component	Part Number	Location and Function
Ducosyn transformer assembly	2007019	SM: Reduces 28 vac to 2 volts and 4 volts for signal generator excitation of accelerometer and gyro ducosyns, respectively.
PIP preamplifier assembly (3)	2007060 2021269	SM: Amplifies signals generated by accelerometer signal generator. Also provides 45 degree phase shift from reference voltage.
Precision resolver alignment assembly	2007001	Outer gimbal resolver intergimbal assembly: Compensates for design anomalies in intergimbal assembly resolvers.
Blower control relay	1010353-10 (system 601 and 602) 1010353-13 (system 603)	Outer gimbal resolver intergimbal assembly: Applies power to blower motors at request of blower control module assembly.

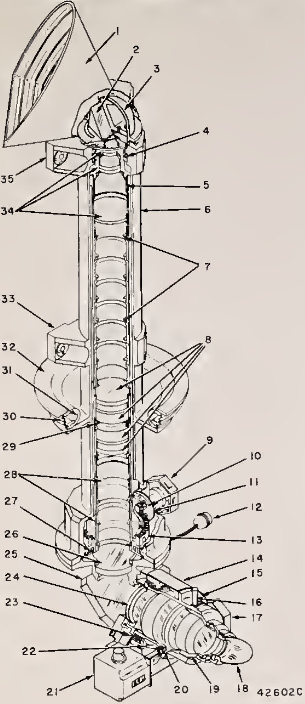
(Sheet 2 of 2)

3-4.5 INTERGIMBAL ASSEMBLIES. The intergimbal assemblies serve five basic purposes: the duplex ball bearings support the gimbal with a minimum of friction, the torque motor drives the gimbal in response to an error signal, the multispeed resolver furnishes signals which represent the angular disposition of the gimbal, the slip rings allow passing of electrical signals from the stable member to the external connectors, and the gyro error resolver (inner gimbal only) transforms gyro error signals into gimbal angle error signals.

3-5 ALIGNMENT OPTICAL TELESCOPE

The AOT (figure 3-5) is a manually operated, periscopic, optical instrument located in the forward structure of the LEM. It is mounted on the nav base with the shaft axis parallel to the LEM X axis, and the upper portion of the shaft protruding from the top of the LEM.

Physically, the AOT is an L-shaped structure formed by the perpendicular intersection of two major assemblies. These assemblies are the telescope shaft and the



1. Sunshade
2. Head prism
3. Head prism housing assembly
4. Ball bearings
5. Inner housing assembly
6. Outer housing assembly
7. Light baffles (7)
8. Relay lenses
9. Shaft positioning knob
10. Shaft positioning gear
11. Detent disc spring
12. P1 connector to CCRD
13. Shaft gear and slotted detent
14. Heater protective cover
15. Worm and gear housing assembly
16. Focus control handle
17. Reticle positioning knob
18. Rubber eyeguard
19. Eyepiece lens assembly
20. Reticle drive worm gear
21. Angle counter and cover
22. Reticle drive gear
23. Ball bearings
24. Reticle and cover ring
25. Mirror
26. Pressure sealing window
27. Ball bearing
28. Light baffles (4)
29. Aperture
30. Flameguard bellows
31. Rubber pressure seal
32. Pressure sealing vehicle mount
33. Nav base and ASA mounting pads (2)
34. Objective lenses
35. Nav base and ASA mounting pads (2)

Figure 3-5. AOT Cutaway View

telescope eyepiece. The major assemblies are jointed by a horizontal flange joint at the base of the telescope shaft assembly. In general, structural components such as housings and mounts are machined beryllium, spacers are aluminum, and threaded parts that engage beryllium are made of corrosion resistant steel. On AOT 6011000-041 and above, a radar shield is mounted on the prism shield plate to keep light reflected by the rendezvous radar antenna from entering the AOT optical system. On AOT's 6011000-073 and -091, the prism shield and radar shield are removed and replaced with the conical sunshade and radar shield assembly (1, figure 3-5) which is attached to the inner housing assembly.

3-5.1 TELESCOPE SHAFT ASSEMBLY. The telescope shaft assembly consists of a stationary outer housing assembly and a rotatable inner housing assembly. It contains the shaft positioning mechanism assembly, most of the AOT optics, and a prism shield.

The inner housing assembly is bearing mounted within the outer housing assembly with the vertical axes of both assemblies coincident. This mounting permits the inner housing assembly to be rotated through 360 degrees about the shaft axis. Six detent positions are provided to lock the shaft at each 60 degrees of rotation. Orientation of the inner housing assembly is accomplished by manually turning the shaft positioning knob (figure 3-5A). By positioning the shaft, the head prism (mounted in a fixed position to the inner housing assembly) is positioned to the desired field of view or behind the protective prism shield.

3-5.1.1 Outer Housing Assembly. The outer housing assembly is a beryllium cylinder approximately 27 inches long with a 3-inch bore diameter and a wall thickness of about 0.100 inch. It houses the shaft positioning mechanism and shaft bearings. The outer wall of the cylinder is flanged to accept the rubber pressure seal and flame guard bellows that interface with the outer wall of the LEM bulkhead. Four machined mounting pads, which are used to mount the AOT to the nav base, extend at right angles from the outer wall of the cylinder.

3-5.1.1.1 Shaft Positioning Mechanism. The shaft positioning mechanism consists of a hexagon knob and bevel gear mounted on a common shaft with a pressure seal interposed between them, and a cantilevered detent disc spring with a ball bearing welded on the free end. The shaft positioning mechanism mates with a bevel gear and slotted detent mounted around the outer periphery of the inner housing assembly. The purpose of the shaft positioning mechanism is to provide a means of manually positioning the optics head prism, attached to the inner housing assembly, to each of three viewing positions and a fourth protective position. Each of the three viewing positions, left (L), forward (F), and right (R), are set 60 degrees from each other while the prism protective position, closed (CL), is set 180 degrees from the forward position. Two additional positions, L_R and R_R, which are not used, are located at 60 degrees on either side of the CL position. A lock is provided at each position by the welded ball bearing as it slides into the 60 degree spaced grooves of the inner housing assembly slotted detent. For AOT's 6011000-073 and -091, the prism shield is removed and all six viewing positions are utilized.

3-5.1.1.2 Prism Shield. The prism shield is attached to the upper end of the outer housing assembly by two bolts on AOT's 6011000-081, 072, and below. All units above

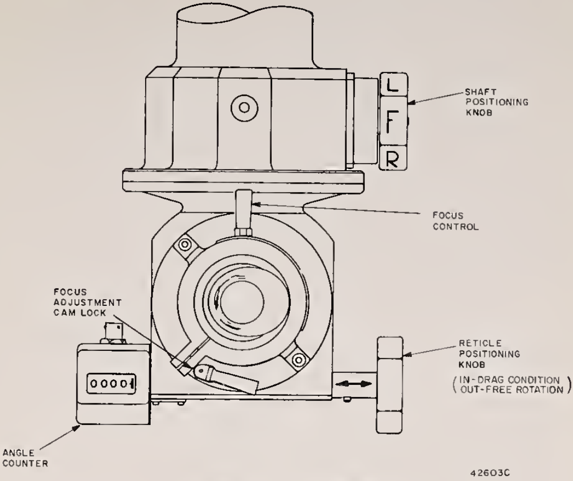


Figure 3-5A. AOT Controls

the 6011000-081 configuration utilize prism shields furnished as GSE. This provides the required protection against damage whenever the conical sunshade and radar shield assembly is not installed. The GSE prism shields, together with the transparent prism and head protection cover, comprise the AOT protective cover set, part number 6014329. This unit primarily functions as a protective shield for the optics head prism against such hazards as micrometeorites, radiation, and dust. The prism shield also acts as part of a labyrinth seal that aids in reducing the evaporation of the shaft ball bearing lubricant. With the head prism facing the rear of the LEM, the shaft closed (CL) position, the prism is completely enclosed by the prism shield. A spacer is mounted between the prism shield and outer housing assembly. This spacer is machined to allow a clearance of only 0.0035 (±0.0015) inch between the inner wall of the prism shield and the head prism mount.

3-5.1.2 Inner Housing Assembly. The inner housing assembly is a beryllium cylinder which is stepped externally to provide seating and retaining surfaces for the shaft ball bearings and internally for seating some of the shaft optics. A bevel gear and slotted detent, used in positioning the inner housing assembly in the previously described viewing and protective positions, is mounted about the lower periphery of the cylinder. Most of the AOT optics are contained within or mounted atop the inner housing assembly. The optics consist of the head prism, objective lenses, relay lenses, and two sets of light baffles. All of the optics are centrally aligned, axially located, and carried in azimuth rotation about the shaft axis with the cylinder. A special wave washer at the lower end of the shaft provides a predetermined load on the shaft ball bearings.

3-5.1.2.1 Head Prism Housing Assembly. The head prism housing assembly, consists of the head prism, prism housing, and prism mount. It is mounted to the objective lens housing assembly on top of the inner housing assembly. The prism housing and mount are machined beryllium and are held to each other by three bolts. The prism, which is inserted between the housing and mount at a 45 degree angle, is held firmly in place by the adjustable force of a leaf spring and epoxy. The leaf spring, located in a recess in the prism housing, is forced to bear down on the rear (hypotenuse) surface of the prism. A U-shaped element, extending upward from the prism mount along the lower face of the prism, acts as a forward retaining surface for the prism. The element also serves as an aperture defining the optics lower field of view. The purpose of the head prism housing assembly is to gather the impinging light rays of the 60 degree field of view. The prism then refracts these rays through a circular passage in the prism mount, concentric with the optical centerline, to impinge on the first element of the objective lens housing assembly.

3-5.1.2.2 Objective Lens Housing Assembly. The objective lens housing assembly, to which the head prism housing assembly is mounted, is mounted to the upper end of the inner housing assembly cylinder by six bolts. The assembly consists of two doublet lenses, the aspherical field lens, spacers, and retaining rings. The retaining rings hold these optics in radial and axial position. The purpose of the objective lens housing assembly is to minify the light rays received from the head prism by 5 power, and focus these rays at the first focal plane of the AOT. The first focal plane is at the exit side of the aspheric field lens.

3-5.1.2.3 Relay Lens Housing Assembly. The relay lens housing assembly is precisely positioned axially inside the stepped lower portion of the inner housing assembly cylinder. The relay lens housing assembly is held in place by a spacer retained against the stepped inner surface of the cylinder above the assembly and below, by a long spacer and a threaded retainer which mates with the lower end of the cylinder. The assembly consists of two identical lens cells and a spacer held together by a threaded coupling ring. The lens cells are power matched and mutually focused. The purpose of the relay lens housing assembly is to collect the minified image light rays from the objective lens housing assembly and focus them at the second AOT focal plane. This focal plane is coincident with the telescope eyepiece assembly reticle in a vacuum environment for AOT 6011000-021 and above, and in an air environment for AOT 6011000-000 and 6011000-011.

3-5.1.2.4 Conical Sunshade and Radar Shield Assembly. The conical sunshade and radar shield assembly is supplied for installation on AOT's 6011000-073 and 6011000-091. The assembly consists of sunshade and radar shield, clamps, shims, and attaching hardware (1, figure 3-5) for attachment to the inner housing assembly. The assembly is shipped and stored in its own shipping container for installation on the AOT after it has been installed on the spacecraft. The function of the assembly is to prevent stray light which is reflected off the skin of the spacecraft and other reflecting surfaces from entering the optics of the AOT. The assembly makes it possible for the astronaut to perform star sightings without having the reflected light blanking out the light emitted from the stars.

3-5.2 TELESCOPE EYEPIECE ASSEMBLY. Mounted on the lower end of the telescope shaft assembly, the telescope eyepiece assembly is the reticle positioning, angle readout, and target-reticle image viewing portion of the AOT. The assembly consists of a mirror and window housing assembly, a worm and gear housing assembly, and a lens housing and eyeguard assembly.

3-5.2.1 Mirror and Window Housing Assembly. The mirror and window housing assembly is a beryllium, 90 degree elbow with two cylindrically flanged ends. It contains an image deflecting mirror and pressure sealing window.

The mirror is machined from 1/2 inch beryllium, heat treated, nickel plated, aluminized, and optically polished. It is mounted in the elbow at 45 degrees to the horizontal eyepiece. This unit provides a means of diverting the target image from the vertical optical centerline of the shaft optics to the horizontal optical centerline of the eyepiece optics.

The window is mounted in a packing ring which is seated in a groove inside the upper portion of the assembly. This unit acts as a seal between the upper AOT components, exposed to the environmental conditions outside the LEM, and the eyepiece optics. Having no optical qualities, the window transmits the target image without change from the relay lens housing assembly directly to the mirror.

3-5.2.2 Worm and Gear Housing Assembly. The worm and gear housing assembly is a beryllium casing containing the reticle and counter drive gear mechanism. AOT reticle, and angle counter. This assembly is mounted to the pressurized end of the mirror and window housing assembly and serves as a mounting receptacle for the eyepiece lens assembly.

The reticle and angle counter drive gear mechanism consists of a transverse worm shaft connected at one end to the angle counter and at the opposite end to the manually operated hexagon control knob. On AOT 6011000-062 and above, the reticle positioning knob has been equipped with a drag mechanism to prevent free rotation of angle counter when hand is removed. (See figure 3-5A.) The worm shaft meshes with the reticle drive gear. This mechanism provides a means of manually positioning the reticle and transmitting that position to the counter where it is read out in terms of angular displacement.

The counter is a continuous readout counter. The counter provides angular readouts from 000.00 degrees to 359.99 degrees. The resolution of the counter is ±0.01

degree (equivalent to ±36 arc seconds). To preclude the possibility of fogging and corrosion, AOT 6011000-062 and above include a hermetically sealed counter with wedge lighting for ease in viewing.

The reticle is positioned at the second focal plane between two plano-plano (glass) discs. The reticle pattern is etched on the surface of one disc and covered by the other disc for protection. The reticle discs are secured with epoxy in a cover ring which is then clamped at three points in the drive gear for planar adjustment. The reticle drive gear, mounted on ball bearings in the housing assembly, provides precision positioning of the reticle in coincidence with the angle counter readout.

In AOT 6011000-021 and above the reticle is positioned so it is in focus under vacuum conditions. The difference in indices of refraction for vacuum and air under normal conditions causes the target to focus at a plane that is not coincident with the reticle when the AOT is used in an earth environment. When in an earth environment, either target or reticle can be brought into focus with the eyepiece, but both cannot be brought into focus simultaneously.

Ten miniature lamps are mounted about the periphery of the reticle to supply the reticle with edge lighting. For AOT 6011000-062 and above, the ten miniature lamps have been painted red to preclude false star indications caused by imperfections in the reticle. A star appears white, while reticle imperfections appear red. To preclude the possibility of fogging because of the presence of moisture and low temperatures, AOT 6011000-021 and above include an electrical heater on the eyepiece assembly. On AOT's 6011000-081 and above, a heater protective cover and reticle lamp protective cover have been installed.

3-5.2.3 Lens Housing and Eyeguard Assembly. The lens housing and eyeguard assembly is a beryllium cylinder containing the eyepiece lens assembly and focusing mechanism, and a rotatable rubber eyeguard. The assembly is inserted into and attached to the worm and gear housing assembly. This assembly is the image exit portion of the AOT.

The eyepiece lens assembly consists of three lens doublets of 5 power. This power is matched to the objective lens power providing an image exit power of unity. The eyepiece lenses are contained in a cylindrical aluminum adapter that is attached to the movable focus control handle. The aluminum adapter moves the eyepiece lenses axially in the housing when driven by the manually operated focus control handle. It thus focuses the viewed image to the exit pupil. The focus control handle protrudes from a helical slot in the lens housing. In AOT 6011000-021 and above, a focus adjustment cam lock (located below and to the left of the eyepiece) can be swiveled, rotating a cam to lock the focus adjustment in a selected position. When the handle is returned to the in-line position, the cam lock is released.

A rotatable eyeguard is fastened to the end of the eyepiece lens assembly. It is made of non-toxic synthetic rubber and is axially adjustable for head position. The adjustment allows for differences in facial contours. The rotatable eyeguard is used when the astronaut takes sightings through the AOT with his face mask opened.

A fixed eyeguard is cemented to the image exit end of the long eye relief (LER) eyepiece lens assembly (figure 3-5B) in AOT 6011000-041 and above. It is made of non-toxic synthetic rubber in an annular shape. The rotatable eyeguard is removed from the AOT when the astronaut takes sightings with his face mask closed. During these sightings, the fixed eyeguard prevents marring of the face mask when pressed against the eyepiece lens assembly.

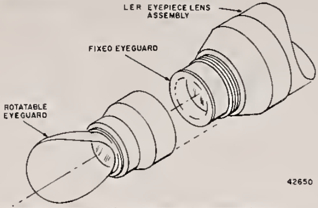


Figure 3-5B. AOT Eyeguard Assemblies

3-5.2.4 AOT High Density Filter Assembly. The AOT high density filter assembly (figure 3-5C) is supplied as a piece of auxiliary equipment to be used in the Apollo mission. The assembly consists of a retainer assembly and high density filter. The retainer assembly contains two lever assemblies mounted on a flexible pivot. The lever assemblies grip the threaded portion of the fixed eyeguard when installed in place of the rotatable eyeguard. (See figure 3-5B.) The function of the assembly is to prevent damage to the astronaut's eyes by accidental direct viewing of the sun.

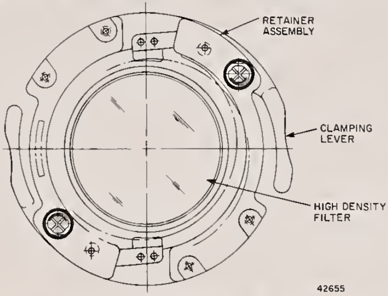


Figure 3-5C. AOT High Density Filter Assembly

3-6 COMPUTER CONTROL AND RETICLE DIMMER ASSEMBLY

The computer control and reticle dimmer assembly (CCRD) (figure 3-6) provides the astronaut the capability of adjusting the brightness of the AOT reticle lamps when taking a star sighting and of marking his target with a MARK-X or MARK-Y pushbutton to obtain the optical angular measurements. The CCRD is approximately 3-3/8 inches high, 4-3/8 inches wide, and 2-1/2 inches deep and weighs approximately three pounds. The CCRD is mounted by means of a bracket to the right side of the AOT eyepiece assembly on PGNCS systems P/N 6015000-041 and below. The CCRD is mounted on the spacecraft AOT guard assembly on PGNCS systems P/N 6015000-051 and above.

Two momentary pushbutton switches, MARK-X and MARK-Y, are used to send discrete signals to the LGC to indicate the time a star crosses the X or Y line on the AOT reticle. A third pushbutton, REJECT, is used to notify the LGC that the previously transmitted mark discrete was incorrect. The pushbuttons are illuminated by a lighting panel consisting of two electro-luminescent lamps.

The reticle dimming circuit consists of a thumbwheel controlled potentiometer which protrudes from the side of the CCRD, two diodes, a control transistor, and a transformer.

The CCRD has two electrical connectors: J1 which mates with the AOT harness and P1 which connects to the LEM harness.

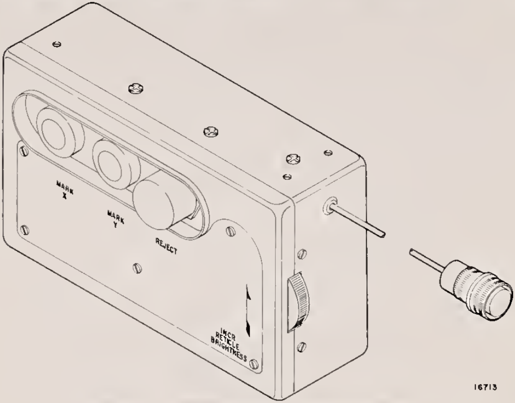


Figure 3-6. Computer Control and Reticle Dimmer

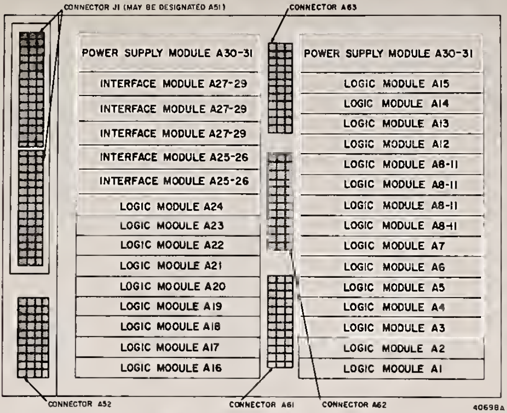


Figure 3-10. Logic Tray A

3-9.1 LOGIC TRAY A. The logic tray A assembly (figure 3-10) contains 31 modules: 24 logic, 5 interface, and 2 power supply modules. All modules are mounted on the tray and then potted with a silastic compound for LGC, part number 2003100, and with a foam for LGC part numbers 2003200 and 2003993. Table 3-VIA gives the part number, function, and location of all modules in logic tray A.

The logic tray A assembly has three intertray connectors (A61, A62, and A63) and two intersystem connectors on the rear. The 360 pin rear connector, J1, connects the LGC to the main 28 vdc power source, to the DSKY, to other components of the PGNCS, and to other LEM systems. The 144 pin rear connector, A52, provides interface with ground support equipment for LGC testing.

LGC's modified by ECP 518 and containing tray A, part number 2003092-041, have wires removed that were used for inhibiting signals STRT1, STRT2, and ALGA; however, the capability for inhibiting STRT1 and ALGA still exists in the GSE.

3-9.2 TRAY B. The tray B assembly (figure 3-11) contains 17 modules, including 6 rope modules. Eleven modules are potted into the tray in a manner similar to that in logic tray A; the six rope modules are plug-in units located at the front of the LGC. The tray B assembly has three intertray connectors (B61, B62, and B63) which interface with those on the logic tray A assembly. Table 3-VIA-1 gives the part number, function, and location of all modules in logic tray B.

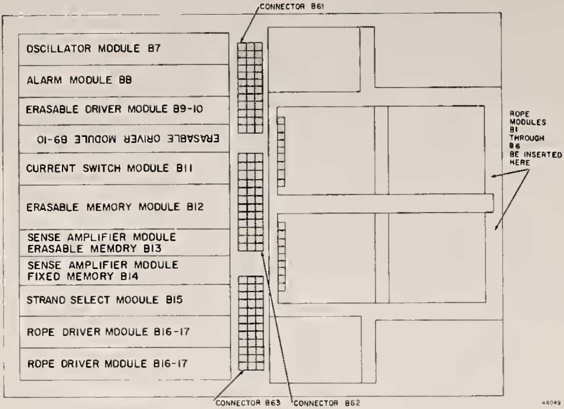

CONNECTOR B61
OSCILLATOR MODULE B7
ALARM MODULE B8
ERASABLE DRIVER MODULE B9-10
ERASABLE DRIVER MODULE B9-10
CURRENT SWITCH MODULE B11
ERASABLE MEMORY MODULE B12
SENSE AMPLIFIER MODULE ERASABLE MEMORY B13
SENSE AMPLIFIER MODULE FIXED MEMORY B14
STRAND SELECT MODULE B15
ROPE DRIVER MODULE B16-17
ROPE DRIVER MODULE B16-17
ROPE MODULES B1 THROUGH B6 BE INSERTED HERE
CONNECTOR B63
CONNECTOR B62
44049

Figure 3-11. Tray B

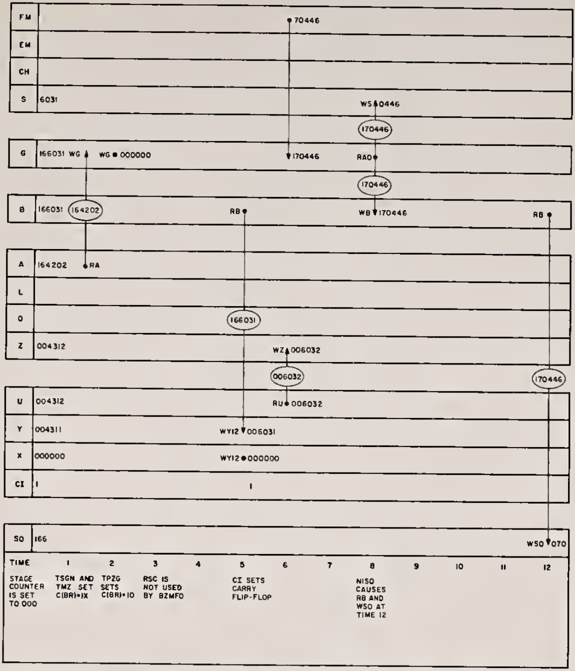


Figure 4-90. Subinstruction BZMF0 with Negative Quantity, Data Transfer Diagram

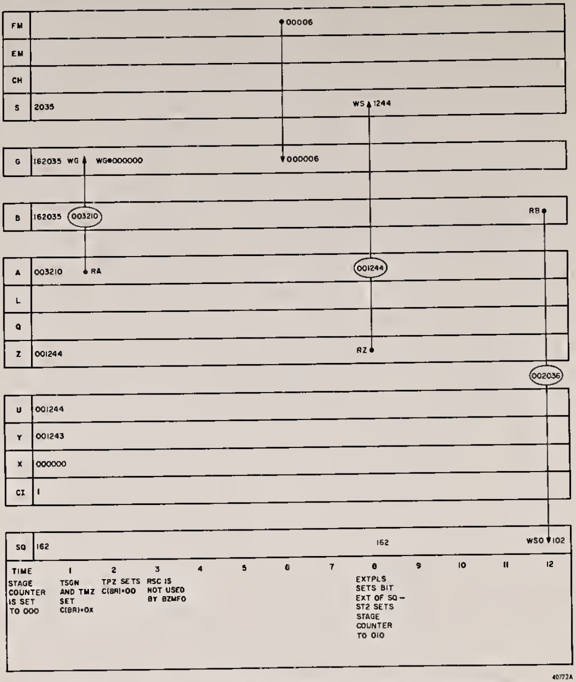


Figure 4-91. Subinstruction BZMF0 with Implied Address Code EXTEND, Data Transfer Diagram

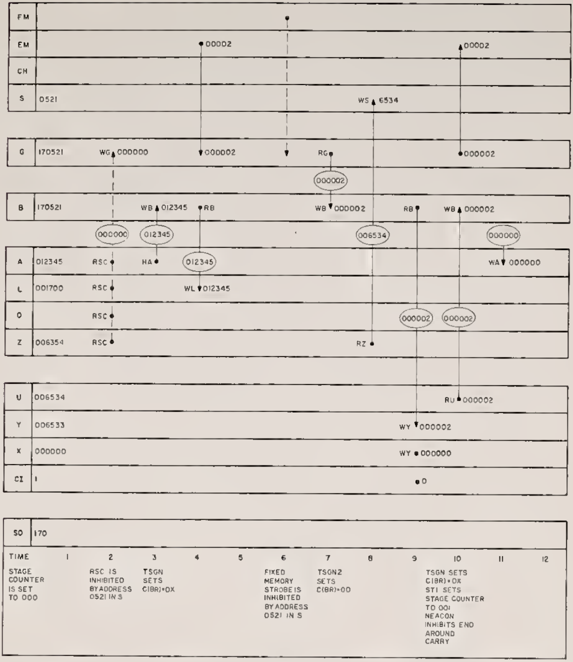


Figure 4-92. Subinstruction MP0 with Two Positive Numbers, Data Transfer Diagram

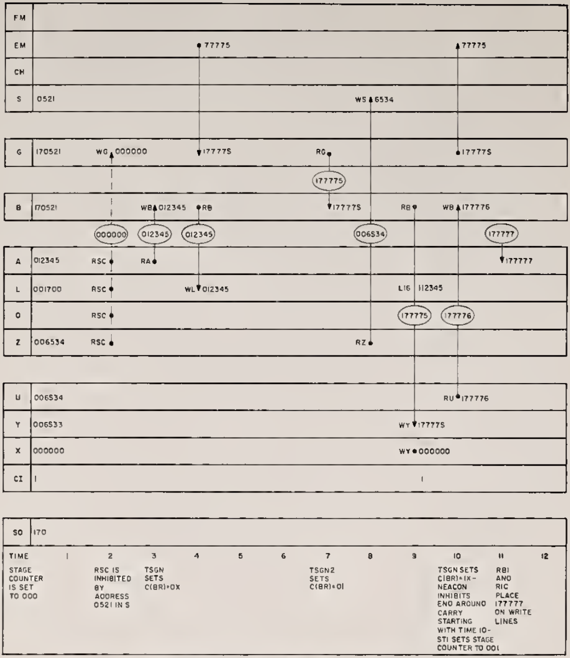


Figure 4-93. Subinstruction MP0 with Positive Number in A and Negative Number in E, Data Transfer Diagram

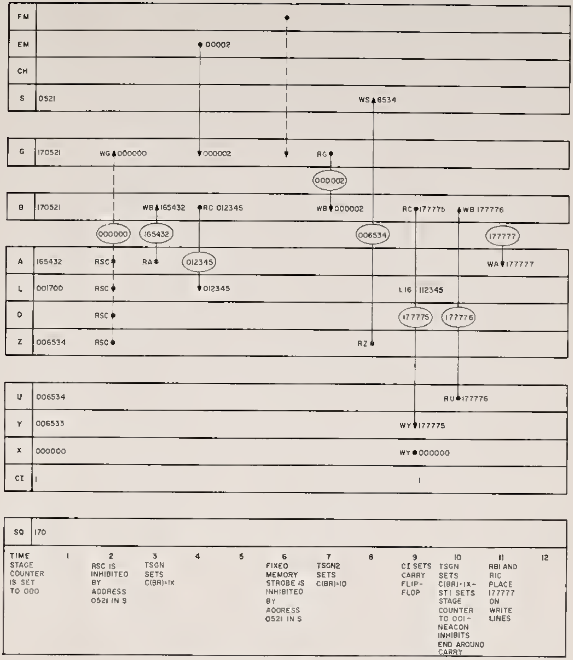


Figure 4-94. Subinstruction MP0 with Negative Number in A and Positive Number in E, Data Transfer Diagram

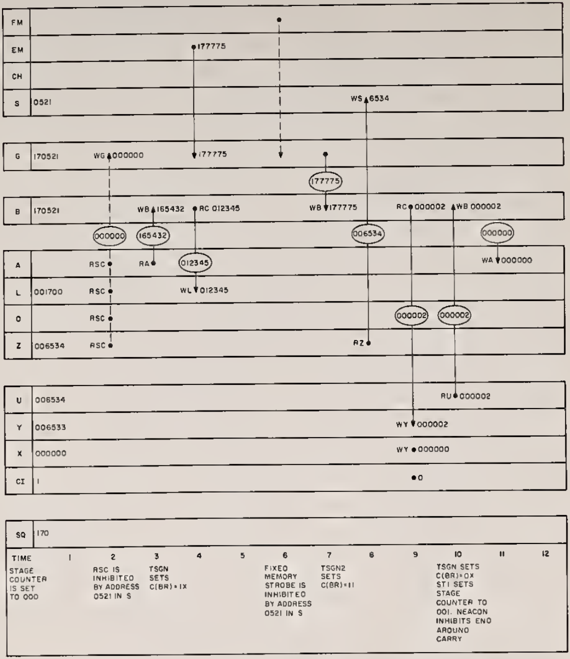


Figure 4-95. Subinstruction MP0 with Two Negative Numbers, Data Transfer Diagram

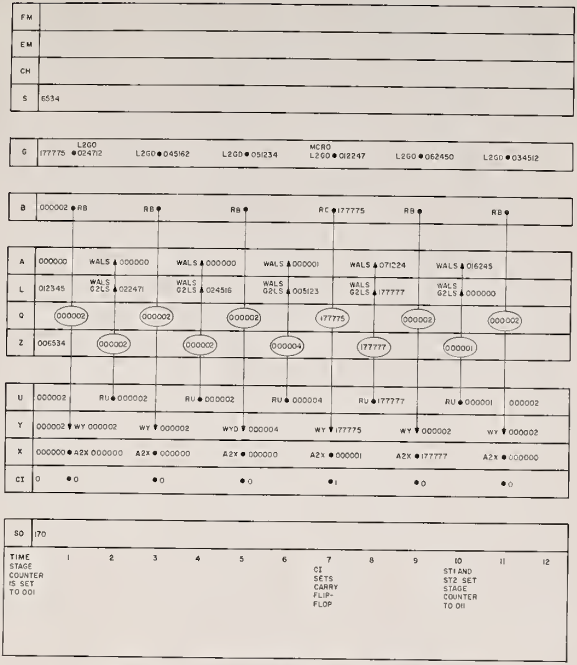
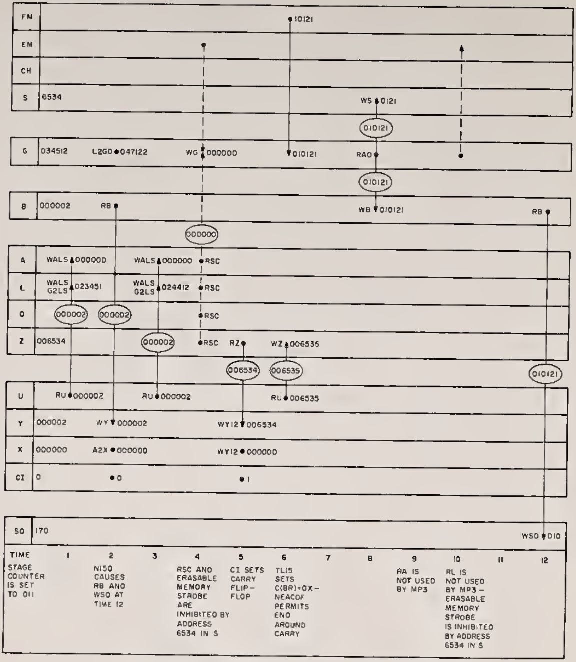

FM
EM
CH
S 6534
G 177775 L2GO ● 024712 L2GO ● 045162 L2GO ● 051234 MCRO L2GO ● 012247 L2GO ● 062450 L2GO ● 034512
B 000002 ● RB RB ● RB ● RC ● 177775 RB ● RB ●
A 000000 WALS ▲ 000000 WALS ▲ 000000 WALS ▲ 000001 WALS ▲ 071224 WALS ▲ 016245
L 012345 WALS G2LS ▲ 022471 WALS G2LS ▲ 024516 WALS G2LS ▲ 005123 WALS G2LS ▲ 177777 WALS G2LS ▲ 000000
Q 000002 000002 000002 177775 000002 000002
Z 006534 000002 000002 000004 177777 000001
U 000002 RU ● 000002 RU ● 000002 RU ● 000004 RU ● 177777 RU ● 000001 000002
Y 000002 ▼ WY 000002 WY ▼ 000002 WYD ▼ 000004 WY ▼ 177775 WY ▼ 000002 WY ▼ 000002
X 000000 ● A2X 000000 A2X ● 000000 A2X ● 000000 A2X ● 000001 A2X ● 177777 A2X ● 000000
CI 0 ● 0 ● 0 ● 0 ● 1 ● 0 ● 0
SQ 170
TIME 1 2 3 4 5 6 7 8 9 10 11 12
STAGE COUNTER IS SET TO 001
CI SETS CARRY FLIP-FLOP
ST1 AND ST2 SET STAGE COUNTER TO 011
40777

Figure 4-96. Subinstruction MP1, Data Transfer Diagram



40778

Figure 4-97. Subinstruction MP3, Data Transfer Diagram

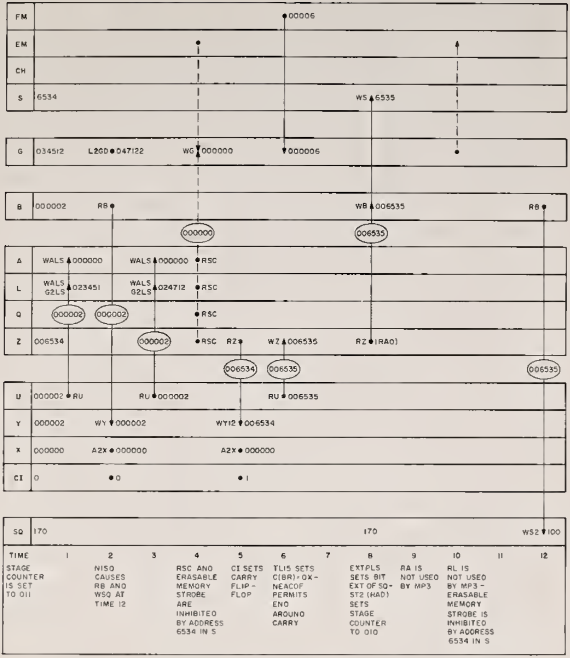


Figure 4-98. Subinstruction MP3 with Implied Address Code EXTEND, Data Transfer Diagram

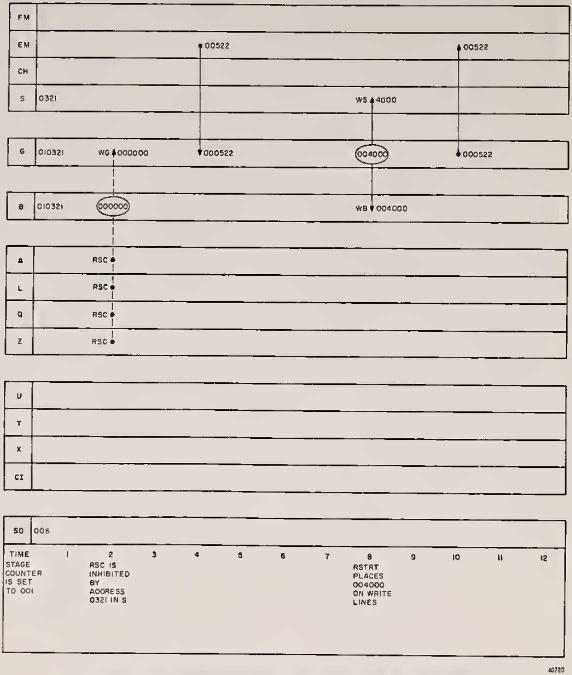


Figure 4-99. Subinstruction GOJ1, Data Transfer Diagram

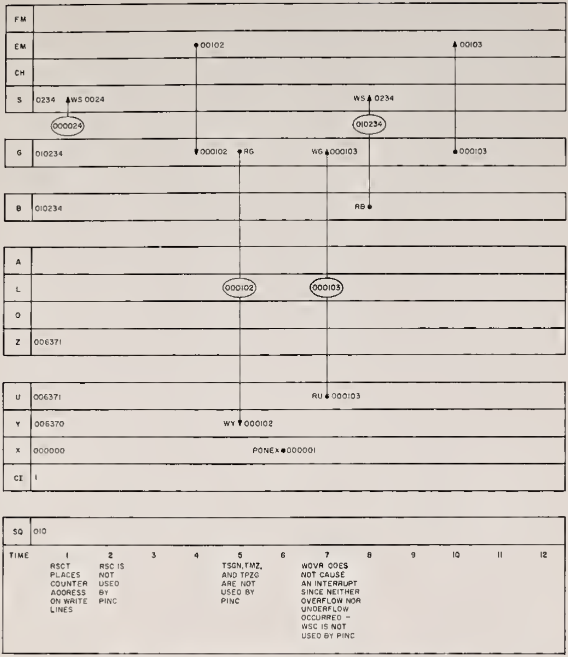


Figure 4-100. Subinstruction PINC, Data Transfer Diagram

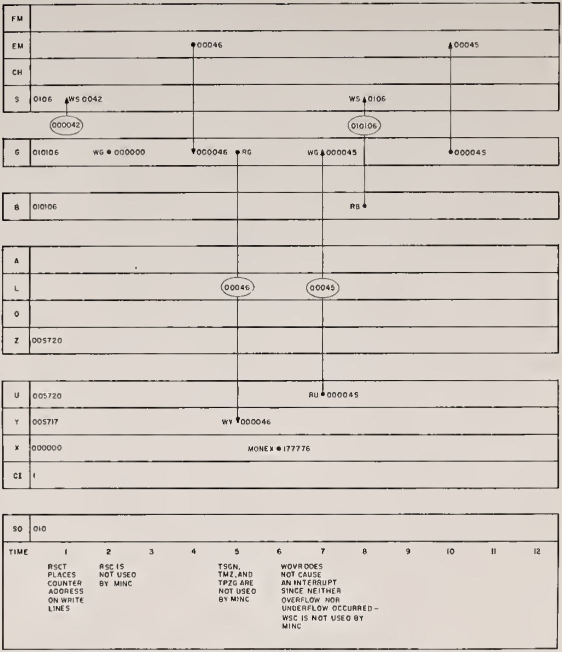


Figure 4-101. Subinstruction MINC, Data Transfer Diagram

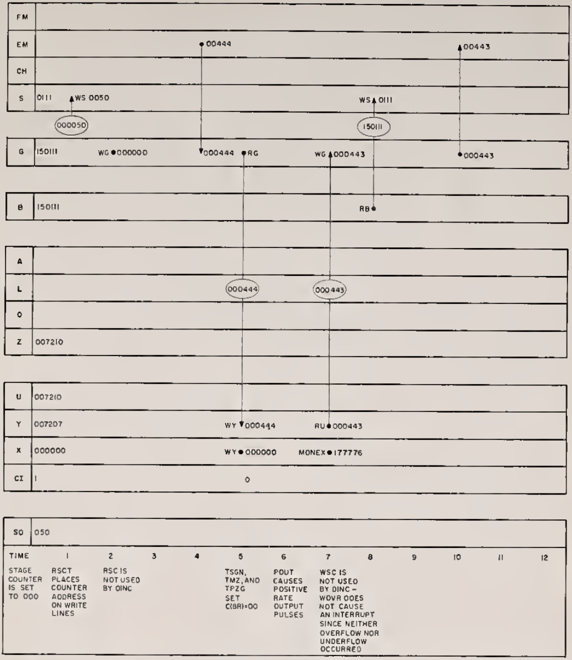

FM
EM
CH
S
G
B
A
L
Q
Z
U
Y
X
CI
SQ
00444
00443
0111
WS 0050
WS 0111
000050
150111
150111
WG 000000
000444
RG
WG 000443
000443
150111
RB
000444
000443
007210
007210
007207
WY 000444
RU 000443
000000
WY 000000
MONEX 177776
1
0
050
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
RSCT PLACES COUNTER ADDRESS ON WRITE LINES
RSC IS NOT USED BY DINC
TSGN, TMZ, AND TPZG SET C(BR)=00
POUT CAUSES POSITIVE RATE OUTPUT PULSES
WSC IS NOT USED BY DINC - WOVR DOES NOT CAUSE AN INTERRUPT SINCE NEITHER OVERFLOW NOR UNDERFLOW OCCURRED
40783

Figure 4-102. Subinstruction DINC with Positive Quantity, Data Transfer Diagram

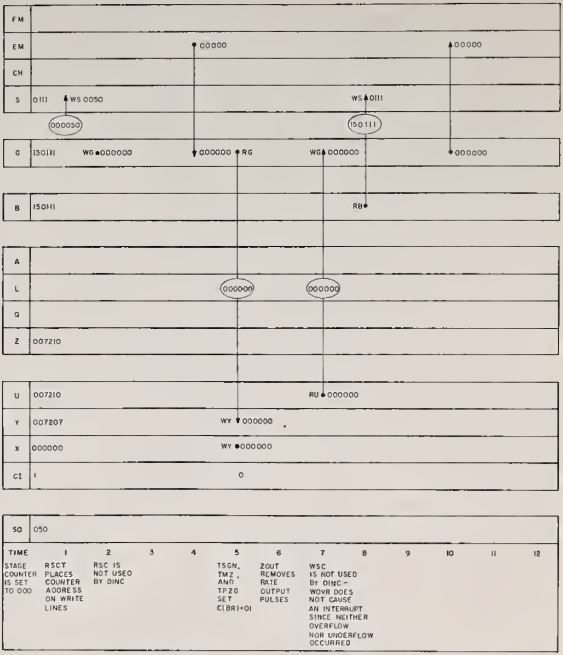

FM
EM
CH
S
G
B
A
L
Q
Z
U
Y
X
CI
SQ
00000
00000
0111
WS 0050
WS 0111
000050
150111
150111
WG 000000
000000
RG
WG 000000
000000
150111
RB
000000
000000
007210
007210
RU 000000
007207
WY 000000
000000
WY 000000
1
0
050
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
RSCT PLACES COUNTER ADDRESS ON WRITE LINES
RSC IS NOT USED BY DINC
TSGN, TMZ, AND TPZG SET C(BR)=01
ZOUT REMOVES RATE OUTPUT PULSES
WSC IS NOT USED BY DINC – WOVR DOES NOT CAUSE AN INTERRUPT SINCE NEITHER OVERFLOW NOR UNDERFLOW OCCURRED
40784

Figure 4-103. Subinstruction DINC with Plus Zero, Data Transfer Diagram

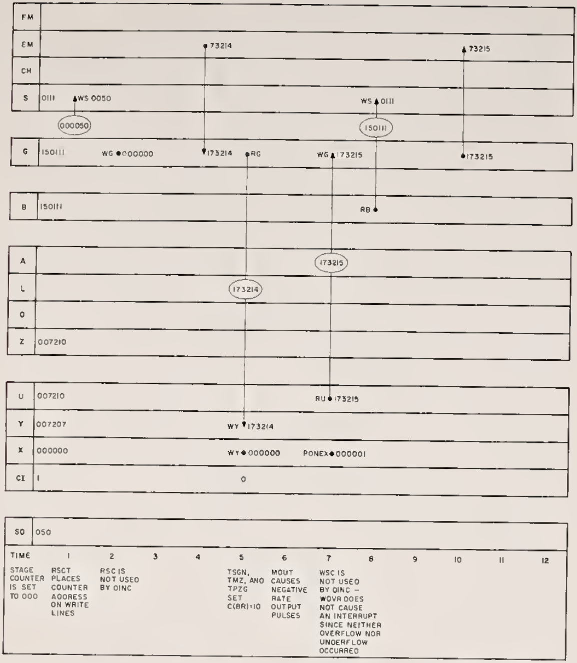

FM
EM
73214
73215
CH
S
0111
WS 0050
WS 0111
000050
150111
G
150111
WG 000000
173214
RG
WG 173215
173215
B
150111
RB
A
173215
L
173214
O
Z
007210
U
007210
RU 173215
Y
007207
WY 173214
X
000000
WY 000000
PONEX 000001
CI
1
0
SO
050
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
RSCT PLACES COUNTER ADDRESS ON WRITE LINES
RSC IS NOT USED BY DINC
TSGN, TMZ, AND TPZG SET C(BR)=10
MOUT CAUSES NEGATIVE RATE OUTPUT PULSES
WSC IS NOT USED BY DINC – WOVR DOES NOT CAUSE AN INTERRUPT SINCE NEITHER OVERFLOW NOR UNDERFLOW OCCURRED
40785

Figure 4-104. Subinstruction DINC with Negative Quantity, Data Transfer Diagram

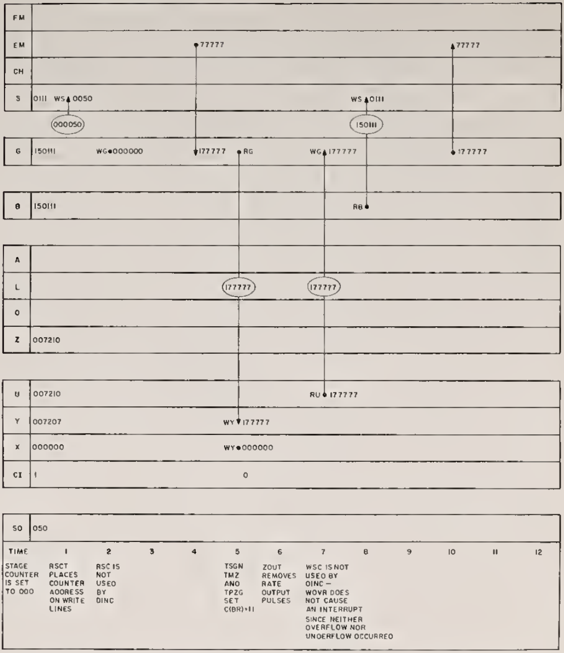

FM
EM
77777
77777
CH
S
0111
WS 0050
000050
WS 0111
150111
G
150111
WG 000000
177777
RG
WG 177777
177777
B
150111
RB
A
L
177777
177777
O
Z
007210
U
007210
RU 177777
Y
007207
WY 177777
X
000000
WY 000000
CI
1
0
SQ
050
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
RSCT PLACES COUNTER ADDRESS ON WRITE LINES
RSC IS NOT USED BY DINC
TSGN TMZ AND TPZG SET C(BR)=11
ZOUT REMOVES RATE OUTPUT PULSES
WSC IS NOT USED BY DINC – WOVR DOES NOT CAUSE AN INTERRUPT SINCE NEITHER OVERFLOW NOR UNDERFLOW OCCURRED
40785

Figure 4-105. Subinstruction DINC with Minus Zero, Data Transfer Diagram

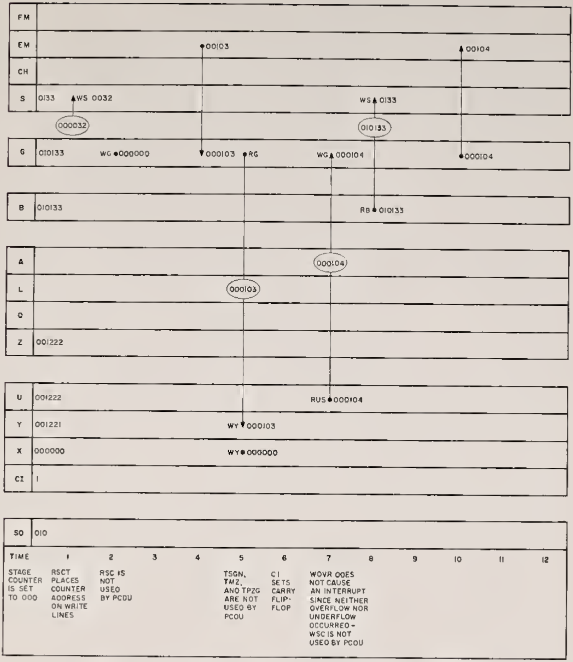


Figure 4-106. Subinstruction PCDU, Data Transfer Diagram

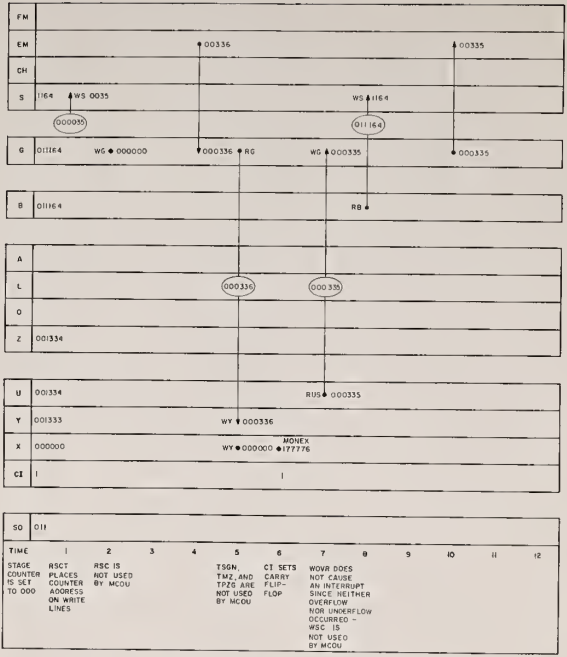


Figure 4-107. Subinstruction MCDU, Data Transfer Diagram

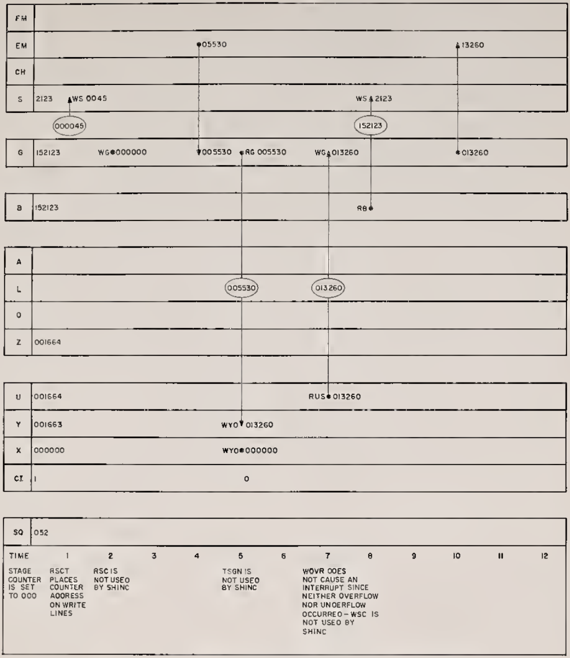


Figure 4-108. Subinstruction SHINC, Data Transfer Diagram

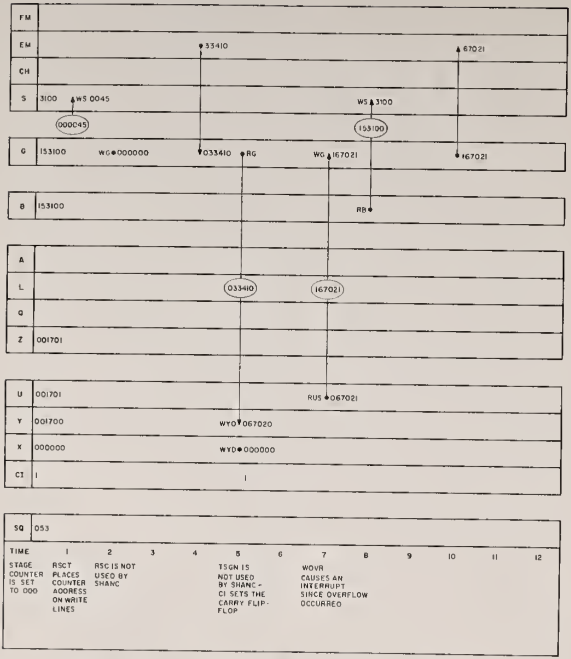


Figure 4-109. Subinstruction SHANC, Data Transfer Diagram

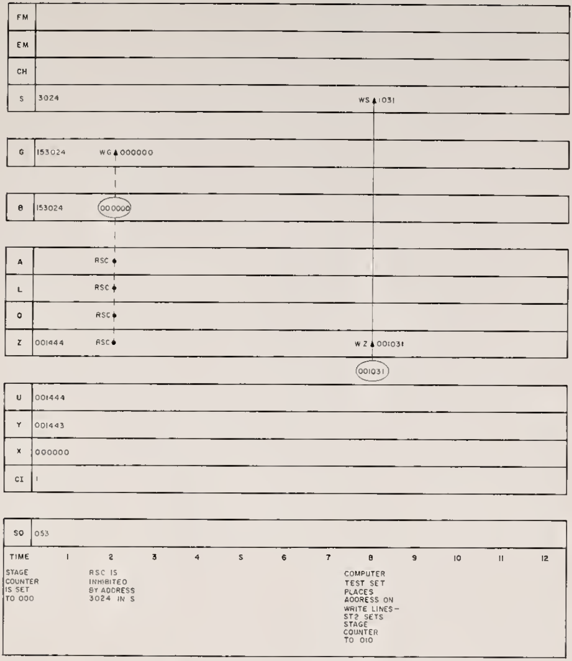

FM
EM
CH
S
3024
WS 1031
G
153024
WG 000000
B
153024
000000
A
RSC
L
RSC
Q
RSC
Z
001444
RSC
WZ 001031
001031
U
001444
Y
001443
X
000000
CI
1
SO
053
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
RSC IS INHIBITED BY ADDRESS 3024 IN S
COMPUTER TEST SET PLACES ADDRESS ON WRITE LINES–ST2 SETS STAGE COUNTER TO 010
40791

Figure 4-110. Subinstruction TCSAJ3, Data Transfer Diagram

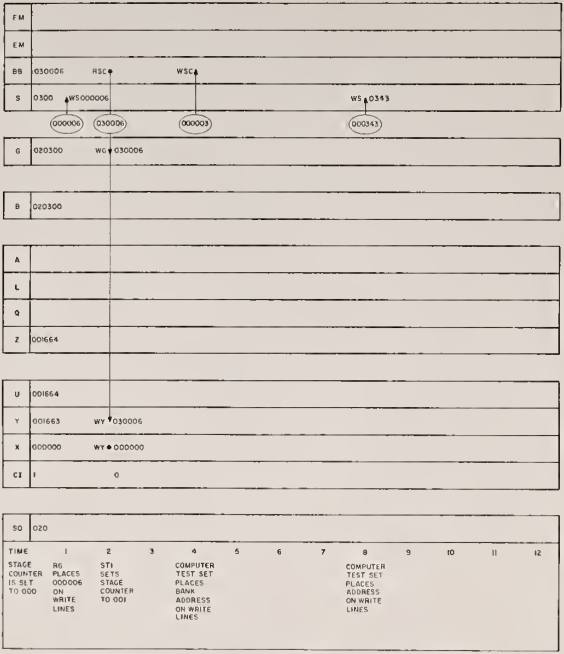

FM
EM
BB
030006
RSC
WSC
S
0300
WS 000006
WS 0343
000006
030006
000003
000343
G
020300
WG 030006
B
020300
A
L
Q
Z
001664
U
001664
Y
001663
WY 030006
X
000000
WY 000000
CI
1
0
SQ
020
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
R6 PLACES 000006 ON WRITE LINES
ST1 SETS STAGE COUNTER TO 001
COMPUTER TEST SET PLACES BANK ADDRESS ON WRITE LINES
COMPUTER TEST SET PLACES ADDRESS ON WRITE LINES
10792

Figure 4-111. Subinstruction FETCH0, Data Transfer Diagram

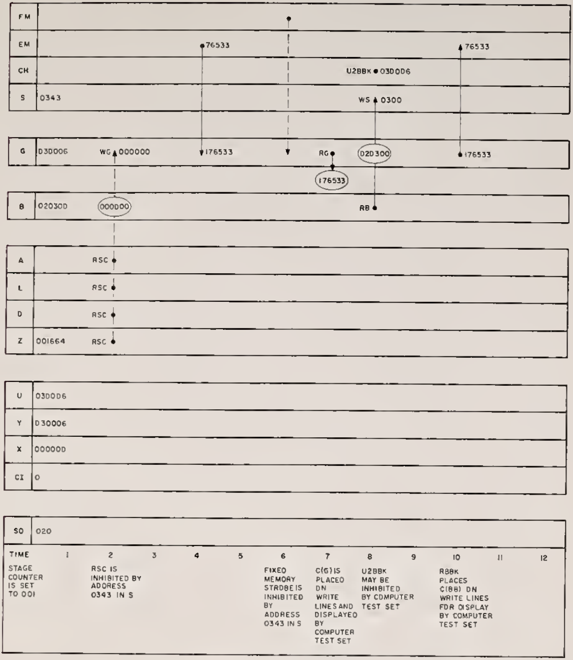
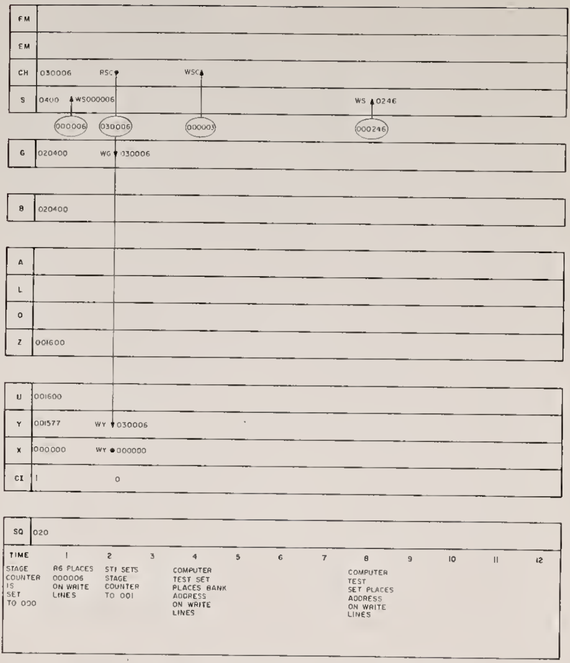

FM
EM
76533
76533
CH
U2BBK 030006
S
0343
WS 0300
G
030006
WG 000000
176533
RG
020300
176533
176533
B
020300
000000
RB
A
RSC
L
RSC
D
RSC
Z
001664
RSC
U
030006
Y
030006
X
000000
CI
0
SO
020
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 001
RSC IS INHIBITED BY ADDRESS 0343 IN S
FIXED MEMORY STROBE IS INHIBITED BY ADDRESS 0343 IN S
C(G) IS PLACED ON WRITE LINES AND DISPLAYED BY COMPUTER TEST SET
U2BBK MAY BE INHIBITED BY COMPUTER TEST SET
RBBK PLACES C(BB) ON WRITE LINES FOR DISPLAY BY COMPUTER TEST SET
40793

Figure 4-112. Subinstruction FETCH1, Data Transfer Diagram


FM
EM
CH
030006
RSC
WSC
S
0400
WS000006
WS 0246
000006
030006
000003
000246
G
020400
WG 030006
B
020400
A
L
O
Z
001600
U
001600
Y
001577
WY 030006
X
000000
WY 000000
CI
1
0
SQ
020
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
R6 PLACES 000006 ON WRITE LINES
STI SETS STAGE COUNTER TO 001
COMPUTER TEST SET PLACES BANK ADDRESS ON WRITE LINES
COMPUTER TEST SET PLACES ADDRESS ON WRITE LINES

40794

Figure 4-113. Subinstruction STORE0, Data Transfer Diagram

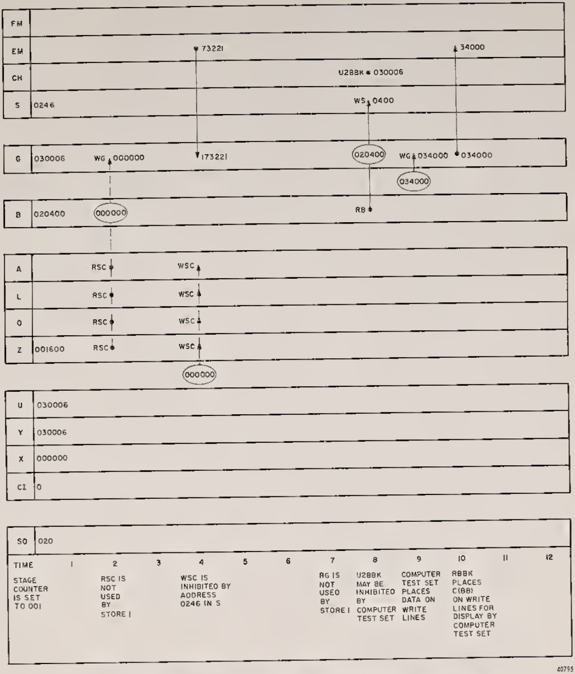

FM
EM
73221
34000
CH
U28BK
030006
S
0246
WS
0400
G
030006
WG
000000
173221
020400
WG
034000
034000
034000
B
020400
000000
RB
A
RSC
WSC
L
RSC
WSC
O
RSC
WSC
Z
001600
RSC
WSC
000000
U
030006
Y
030006
X
000000
CI
0
SO
020
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 001
RSC IS NOT USED BY STORE I
WSC IS INHIBITED BY ADDRESS 0246 IN S
RG IS NOT USED BY STORE I
U28BK MAY BE INHIBITED BY COMPUTER TEST SET
COMPUTER TEST SET PLACES DATA ON WRITE LINES
RBBK PLACES C(BB) ON WRITE LINES FOR DISPLAY BY COMPUTER TEST SET
40795

Figure 4-114. Subinstruction STORE1, Data Transfer Diagram

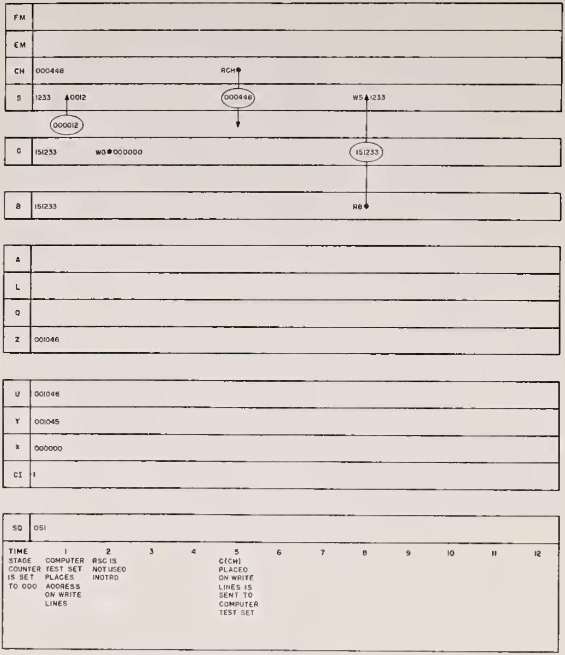


Figure 4-115. Subinstruction INOTRD, Data Transfer Diagram

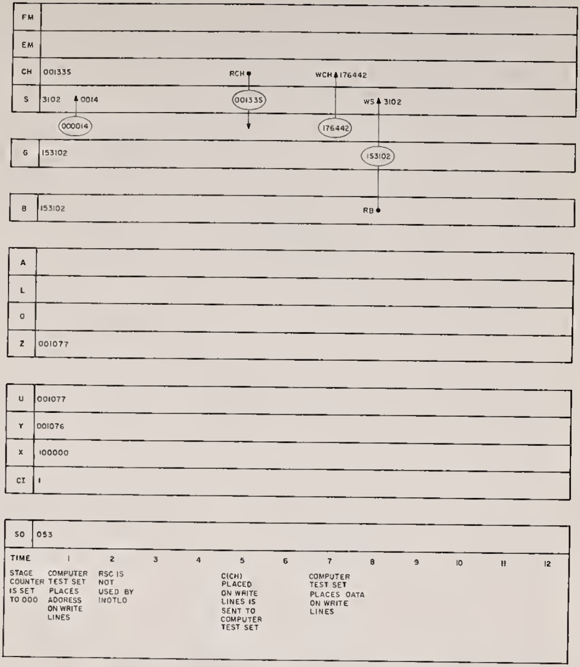

FM
EM
CH
001335
RCH
WCH
176442
S
3102
0014
000014
001335
176442
WS
3102
G
153102
153102
B
153102
RB
A
L
Q
Z
001077
U
001077
Y
001076
X
100000
CI
1
SQ
053
TIME
1
2
3
4
5
6
7
8
9
10
11
12
STAGE COUNTER IS SET TO 000
COMPUTER TEST SET PLACES ADDRESS ON WRITE LINES
RSC IS NOT USED BY INOTLD
C(CH) PLACED ON WRITE LINES IS SENT TO COMPUTER TEST SET
COMPUTER TEST SET PLACES DATA ON WRITE LINES
40797

Figure 4-116. Subinstruction INOTLD, Data Transfer Diagram

4-5.3 TIMER. The timer generates all timing functions required for operation of the computer. In addition, the timer is the primary source of all timing and sync signals for all the spacecraft systems.

4-5.3.1 Timer Functional Description. Timer operation contains the functional areas indicated in figure 4-117. These functional areas include the oscillator, clock divider logic, scaler, time pulse generator, and the sync and timing logic. The oscillator is a crystal controlled, modified Pierce oscillator design that generates a source frequency of 2.048 mc for the clock divider logic. Temperature compensated components in the oscillator circuit maintain a high degree of stability and assure an extremely accurate output frequency to the clock divider logic.

The clock divider logic is further subdivided into the main clock divider, ring counter, and strobe pulse generator. The 2.048 mc input from the oscillator is applied to the main clock divider. The main clock divider divides the input frequency by two and generates the following outputs: clear, write, and read control pulses (CT, $\overline{\text{WT}}$, $\overline{\text{RT}}$) which are applied to the central processor to produce the signals necessary to clear, write into, and read out the flip-flop registers; 1.024 mc gating pulses ($\overline{\text{PHS2}}$, $\overline{\text{PHS3}}$, $\overline{\text{PHS4}}$, $\overline{\text{OVFSTB}}$, $\overline{\text{TT}}$) which are used throughout the computer; the master clock signal (CLK), a 1.024 mc output used to synchronize the other spacecraft systems; and signal Q2A which is applied to the oscillator alarm circuit in the power supply to indicate oscillator activity. In addition, the main clock divider supplies signals ($\overline{\text{RING A}}$ and $\overline{\text{RING B}}$) to drive the ring counter, and signals ($\overline{\text{EVNSET}}$ and $\overline{\text{ODDSET}}$) to the time pulse generator. These latter outputs occur at a 512 kc rate, a result of further division of the 1.024 mc gating rate within the main clock divider.

The ring counter generates outputs (P01 through P05) at a 102.4 kc rate. The outputs are 5 microsecond pulses used for gating and for deriving other timing functions in the computer. Ring counter outputs are also used to derive the strobe pulses (SB0, SB1, SB2, SB4) from the strobe pulse generator. These outputs also occur at a 102.4 kc rate and are 3 microseconds in width with the exception of SB4, which is a 2 microsecond pulse.

The scaler consists of 33 identical divider stages. The stages are cascaded so that the frequency division is successive. The first stage, driven by signal $\overline{\text{P01}}$ from the ring counter, generates outputs at a rate of one-half the input or 51.2 kc. This output and the remaining outputs through stage 17 (0.78125 pps) are used for timing and gating. The outputs appear as signal outputs from flip-flop circuits (FS01, etc.), and 10 microsecond pulse outputs (F01A, etc.) at the same frequency as the associated stage. Stages 6 through 19 and 20 through 33 form a 28 bit real time word (CHAT01 through CHAT14, CHBT01 through CHBT14) which indicates time intervals up to 23.3 hours.

The time pulse generator, consisting of 12 flip-flop circuits, generates timing pulses $\overline{\text{T01}}$ through $\overline{\text{T12}}$. This sequence of timing pulses defines one MCT within the LGC, or a period of 11.97 microseconds, in which word flow takes place. The time pulse generator is driven by inputs ($\overline{\text{EVNSET}}$ and $\overline{\text{ODDSET}}$) from the main clock divider.

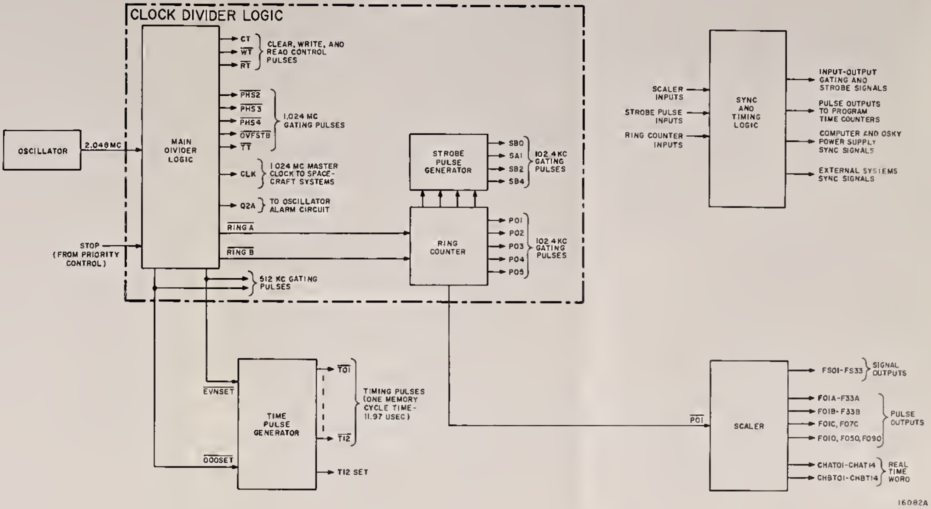


Figure 4-117. Timer, Functional Diagram

Signal $\overline{\text{ODDSET}}$ can be inhibited by signal STOP from priority control. Signal STOP, an input from the CTS during preinstallation system and subsystem tests, inhibits the time pulses from being generated thus preventing word flow in the computer. This feature allows individual memory cycle times to be observed during tests.

The sync and timing logic consists of a gating complex which generates various outputs for use within the computer, and synchronization signals for systems external to the computer. The inputs to, and outputs from, this section are extensive, and are grouped by function in figure 4-117.

The ring counter, strobe pulse generator, and the scaler supply inputs to the sync and timing logic. These inputs are used to derive gating and strobe signals for the input and output channels, pulse outputs for the program time counters in memory, and synchronization signals for the computer and DSKY power supplies and for systems external to the computer.

During standby operation, the oscillator, clock divider logic, and the scaler are operative and generate the signals associated with these functional areas. However, the significant outputs during this mode of operation are the real time word from the scaler and the synchronization signals to the other spacecraft systems. The real time word continues to be accumulated during standby, and the external systems synchronization signals continue to be generated.

4-5.3.2 Oscillator Detailed Description. The computer oscillator (figure 4-118) generates a master clock frequency of 2.048 mc. The basic oscillator circuit, consisting of crystal Y1, and transistor Q1 and associated components, is a modified Pierce oscillator design. Variable inductor L1, in series with the crystal, compensates for frequency drift due to component aging. The crystal output is amplified by transistor Q1, which operates as a class A amplifier that drives buffer stage Q2. The sinusoidal output of stage Q2 is applied to pulse shaper Q3 and, through capacitor C7, to a dc feedback network. The output of the feedback network controls the peak-to-peak output level of stage Q1. The resultant 2.048 mc square wave output of stage Q3 is amplified by output stage Q4, and is applied to the clock divider logic.

The collector supply voltage for stages Q1 and Q2 is obtained from the +14 volt output (B PLUS) of the power supply. This voltage is applied through resistor R5 and is regulated by zener diode CR1 (rated at 9 volts). The +4 volt power supply output is furnished directly as the collector supply for stages Q3 and Q4.

Two resistor networks (R4, R6, R10, R9, R12 and R2, R3, R7, R8, R11), in conjunction with thermistors RT1, RT2, and RT3 and varicap CR2, comprise the temperature compensation network which improves the stability of the computer oscillator. The regulated output voltage of diode CR1 is applied across the two resistor networks, the outputs of which are applied across varicap CR2. The varicap is a reverse-biased diode that introduces capacitance into the circuit. Any changes in temperature cause a corresponding change in the reverse bias across the varicap thus varying the effective capacitance in series with crystal Y1, which is also affected by the change in temperature.

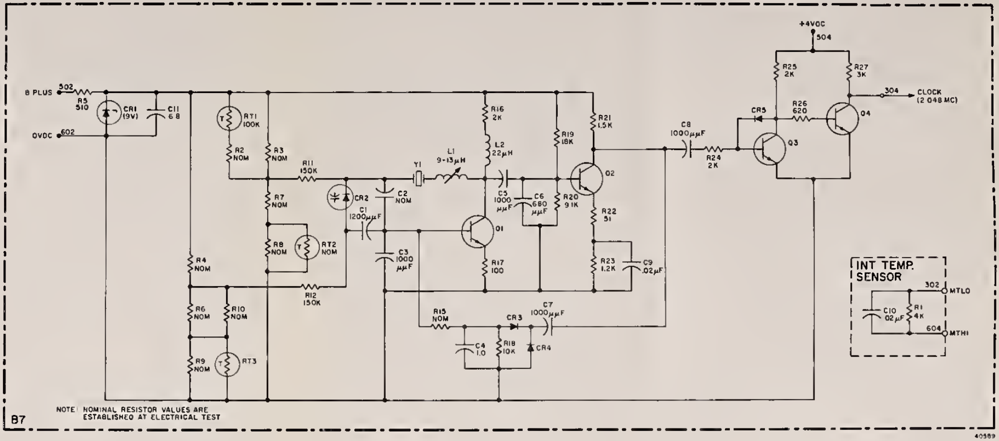


Figure 4-118. Computer Oscillator, Schematic Diagram

4-5.3.3 Clock Divider Logic Detailed Description. The clock divider logic consists of the main clock divider, ring counter, and strobe pulse generator. The main clock divider (figure 4-119, sheet 1) generates outputs at the basic clock rate of the system, 1.024 mc. In addition, 512 kc outputs drive the ring counter and the time pulse generator. The 2.048 mc CLOCK input from the oscillator is applied to the first main clock divider circuit consisting of gates 37101 through 37106. Gates 37101 through 37104 are interconnected in a manner similar to the basic flip-flop circuit of the LGC. Gates 37105 and 37106 function as a flip-flop; however, gates 37101 through 37104 do not. The waveforms in figure 4-119 indicate that an output occurs from only one of the four gates at each positive and negative transition of the clock input. The other three gates remain in ZERO state. Unlike a flip-flop, in which one side is ZERO while the other side is a ONE and vice-versa, this circuit resembles a ring counter. The outputs of these four gates (37101 through 37104) are used to derive the clear control signal ($\overline{\text{CT}}$), read control signal ($\overline{\text{RT}}$), and the three 1.024 mc gating pulses ($\overline{\text{PHS2}}$, $\overline{\text{PHS3}}$, and $\overline{\text{PHS4}}$) which are 0.25 microseconds wide.

The outputs from gates 37102 and 37103 drive FF37105-37106, which is alternately set and reset at 1.024 mc rate. The write control signal ($\overline{\text{WT}}$) and the 1.024 mc master clock (CLK) signal to the spacecraft systems are derived from this flip-flop output. Any failure of the computer oscillator would be most directly indicated by the output of the first main clock divider circuit. Thus, signal Q2A is applied to the oscillator alarm circuit in the power supply to indicate oscillator activity. The output is from an extended NOR gate which has its collector load in the alarm circuit. Figure 4-119 illustrates the timing relationship between the clear and write control signals. The 0.25 microsecond clear pulse is coincident with the first 1/4 microsecond of the 0.5 microsecond write control signal. The read control signal is 0.75 microsecond wide. All three of these control signal outputs are applied to the central processor for clearing, writing into, and reading out of the flip-flop registers. The clear pulse (CT) is used also to derive the overflow strobe signal ($\overline{\text{OVFSTB}}$), a 1.024 mc gating signal. This output is shown wider than the clear pulse since some propagation delay undoubtedly exists to stretch this pulse slightly beyond 0.25 microsecond before FF37148-37149 resets.

The inverted output of gate 37101 drives the second main clock divider circuit which consists of gates 37111 through 37114 and FF37117-37118. Outputs from this circuit drive the ring counter ($\overline{\text{RING A}}$, $\overline{\text{RING B}}$) and the time pulse generator ($\overline{\text{ODDSET}}$, EVNSET). The outputs occur at a 512 kc rate, and are 90 degrees out of phase with each other (see figure 4-119). This main clock divider circuit is identical in operation to the first main clock divider circuit. Each of the gates 37111 through 37114 generates in succession an output on each transition of the output of gate 37107. Output pulses from gates 37112 and 37113 alternately set and reset FF37117-37118. No output signals are derived from this flip-flop. The outputs to drive the ring counter and the time pulse generator are obtained from gates 37111 and 37114. Signals $\overline{\text{RING A}}$ and ODDSET from 37111 occur coincidentally, and $\overline{\text{RING B}}$ and $\overline{\text{EVNSET}}$ from 37114 occur coincidentally. Signal $\overline{\text{ODDSET}}$, applied to the time pulse generator, can be inhibited by input STOP from priority control, which prevents any outputs from the time pulse generator and subsequently inhibits word flow in the computer. This feature can be

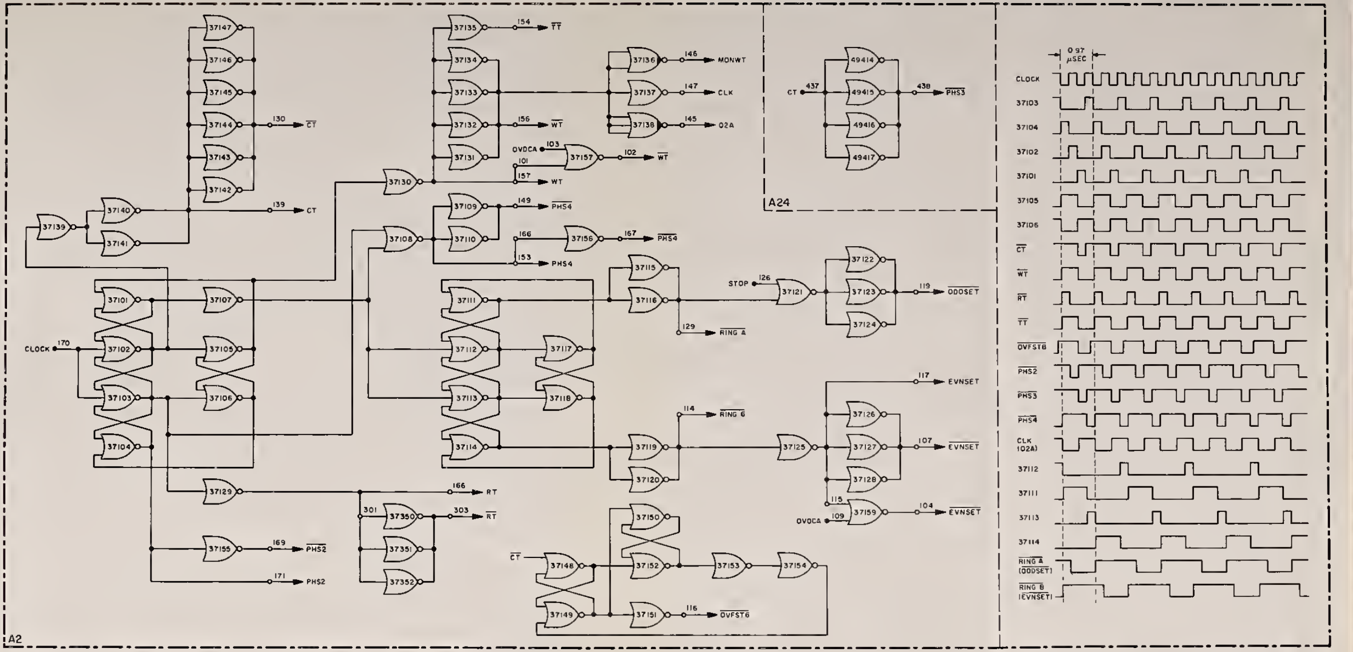


Figure 4-119. Clock Divider Logic
(Sheet 1 of 2)

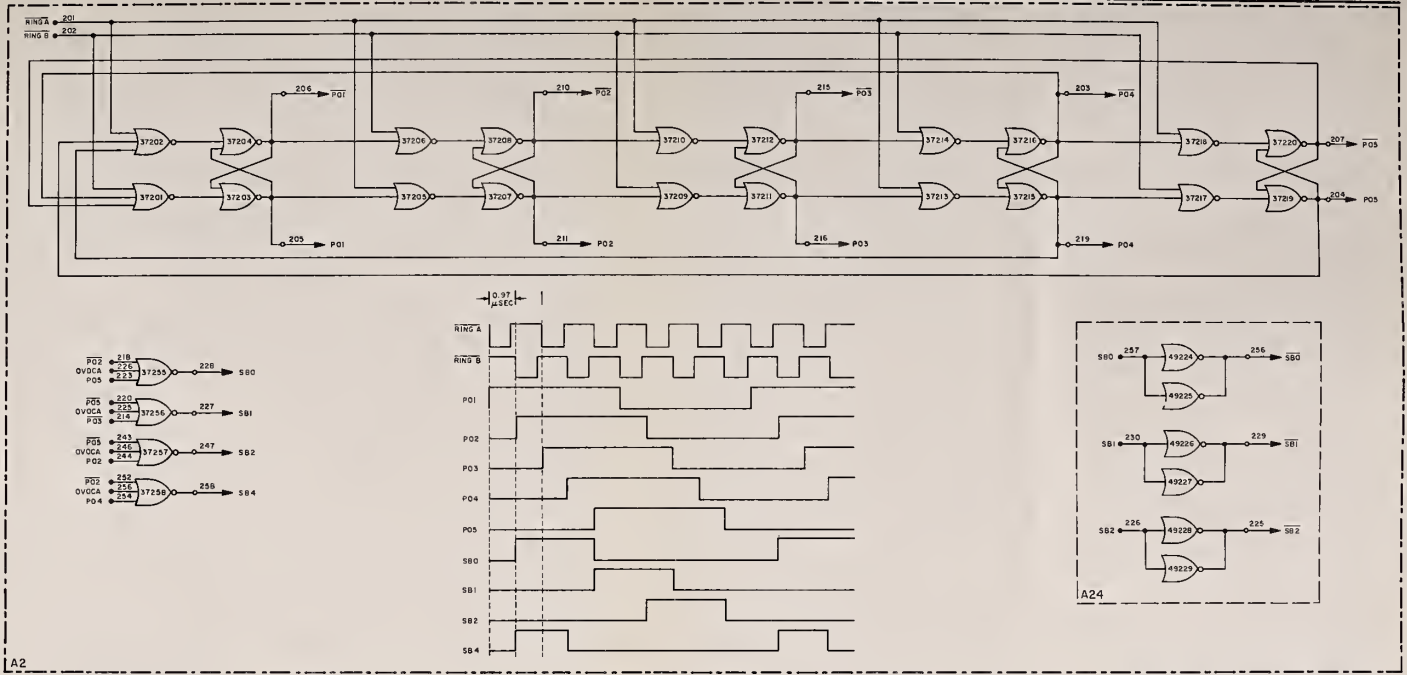


Figure 4-119. Clock Divider Logic
(Sheet 2 of 2)

employed during pre-installation system and subystem tests as a result of a monitor stop (MSTP) input from the CTS.

The ring counter (figure 4-119, sheet 2) consists of five flip-flop circuits with outputs labeled P01 through P05 (and $\overline{\text{P01}}$ through $\overline{\text{P05}}$). The ring counter is driven by inputs ($\overline{\text{RING A}}$ and $\overline{\text{RING B}}$) from the main clock divider. Each of these inputs, described previously, occurs at a 512 kc rate. The ring counter does not accomplish a division-by-two. Rather, the division by the fives stages results in five symmetrical outputs, each at a rate of 102.4 kc and 5 microseconds in width. Successive outputs occur 1 microsecond apart; for example, P02 occurs 1 microsecond after P01 etc.

Strobe pulses SB0, SB1, SB2, and SB4 are generated by signals P02 through P05 (and complements) from the ring counter. These strobes are 3 microsecond pulses occurring also at a rate of 102.4 kc, (with the exception of SB4 which is 2 microseconds wide). Strobe signals SB0, SB1, and SB2 are inverted by gates on module A24 (see figure 4-119).

4-5.3.4 Scaler Detailed Description. The scaler, figure 4-120, consists of 33 identical divider stages. The stages are cascaded to provide successive frequency division of the input to the scaler. Stage 2 runs at half the rate of stage 1, stage 3 at half the rate of stage 2, etc. Each of these stages is identical in operation to the main clock divider circuit in the clock divider logic. The input to the scaler, signal $\overline{\text{P01}}$ from the ring counter, occurs at a rate of 102.4 kc. It is applied to stage 1 located on module A2 (the remaining stages of the scaler are located on module A1). Stage 1 divides this input by two and generates outputs at a rate of 51.2 kc. There are five outputs available from stage 1): four pulse outputs (F01A through F01D) from the input gates (37221 through 37224), and one flip-flop output (FF37225-37226).

The pulse outputs of stage 1 are 5 microseconds wide. The period of the flip-flop output is approximately 20 microseconds; since the output waveform is symmetrical, the transitions are 10 microseconds apart. The output of the stage 1 flip-flop is the input to stage 2 of the scaler. Stage 2 divides the input by two and generates outputs at a rate of 25.6 kc. Three outputs are available from stage 2: two pulse outputs (F02A, F02B), and the flip-flop output (FS02). The pulse outputs of this stage and all subsequent stages of the scaler, regardless of frequency, are 10 microseconds wide. This width is established by the 10 microsecond input from stage 1 to stage 2 and the fact that a pulse output, not the flip-flop output, feeds stage 3 (F02A). The same is true of the output from stage 3 to stage 4 (F03A) and of the succeeding scaler stages.

Figure 4-121 illustrates the output waveforms from stages 1 and 2 of the scaler. The outputs from stage 2 are typical of the outputs from the remaining stages of the scaler, with the exception of stages 5, 7, and 9. Stages 5 and 9 have one additional pulse output (F05D, F09D) and stage 7 two additional pulse outputs ($\overline{\text{F07C}}$, $\overline{\text{F07D}}$). These outputs are generated by gates on module A24 as indicated in figure 4-120.

Most of the pulse outputs designated A and B, which are positive going, are inverted by gates contained in other modules. These gates, and the modules in which they are located, are also illustrated in figure 4-120.

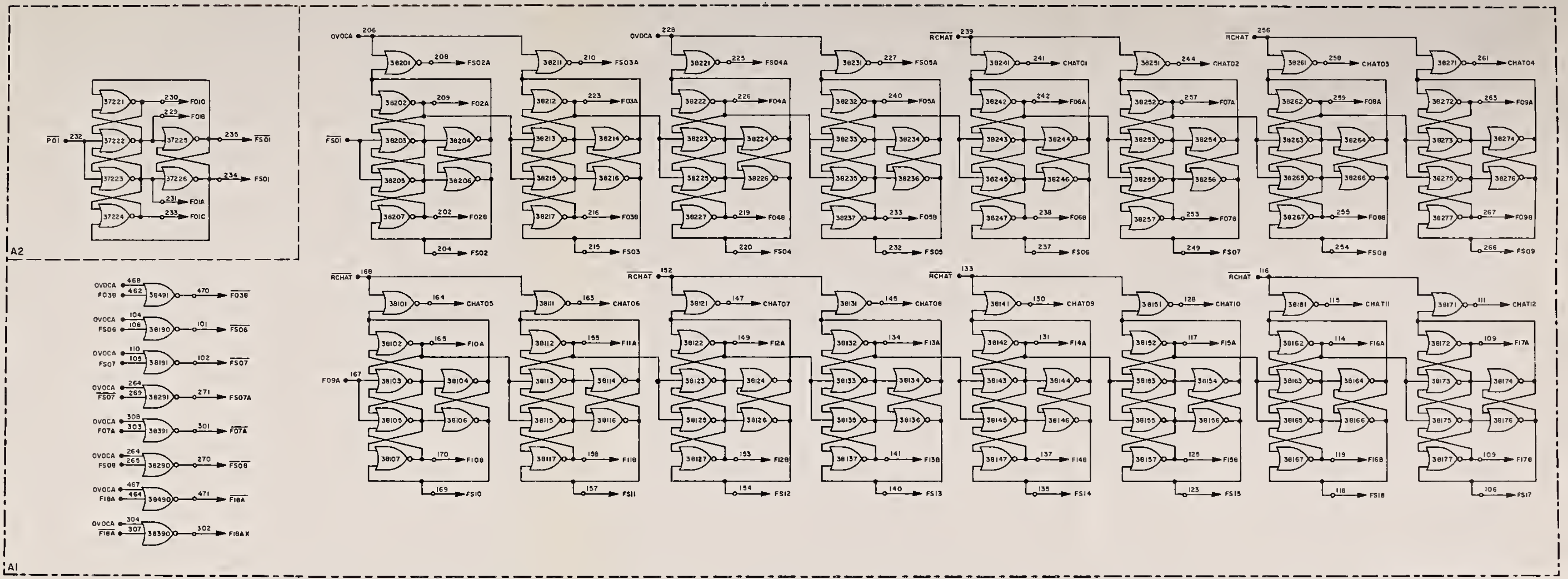


Figure 4-120. Scaler (Sheet 1 of 2)

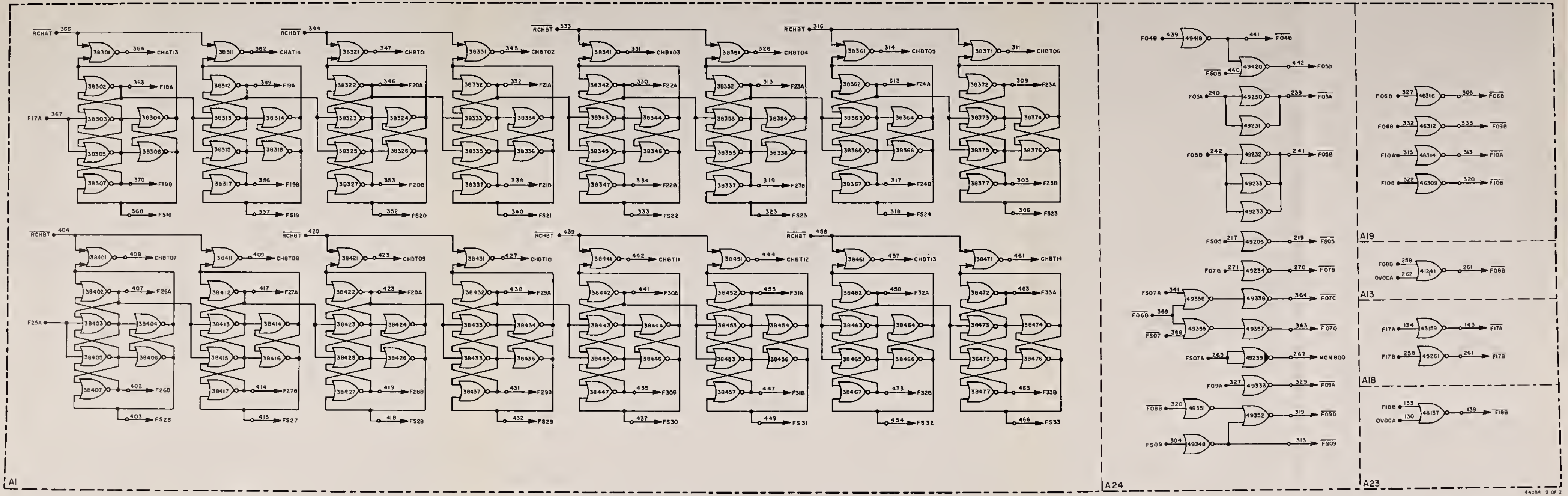
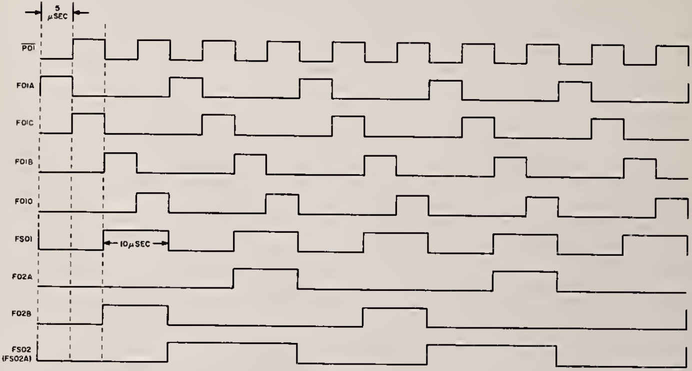


Figure 4-120. Scaler (Sheet 2 of 2)



NOTE: THE OUTPUTS OF STAGE 2 (FS02, FO2A, FO2B) ARE TYPICAL OF THE OUTPUTS (EXCLUDING FREQUENCY) FROM THE REMAINING STAGES OF THE SCALER

40592A 1 of 3

Figure 4-121. Scaler Waveforms (Sheet 1 of 3)

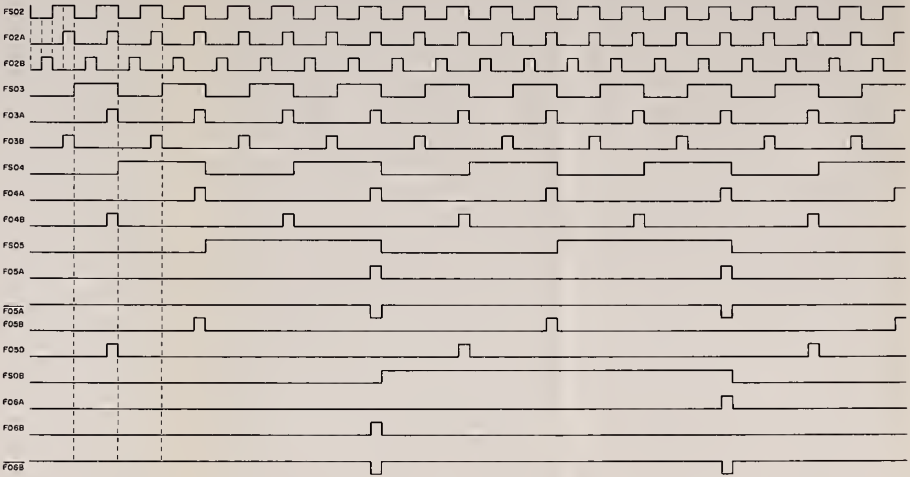


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Figure 4-121. Scaler Waveforms
(Sheet 2 of 3)

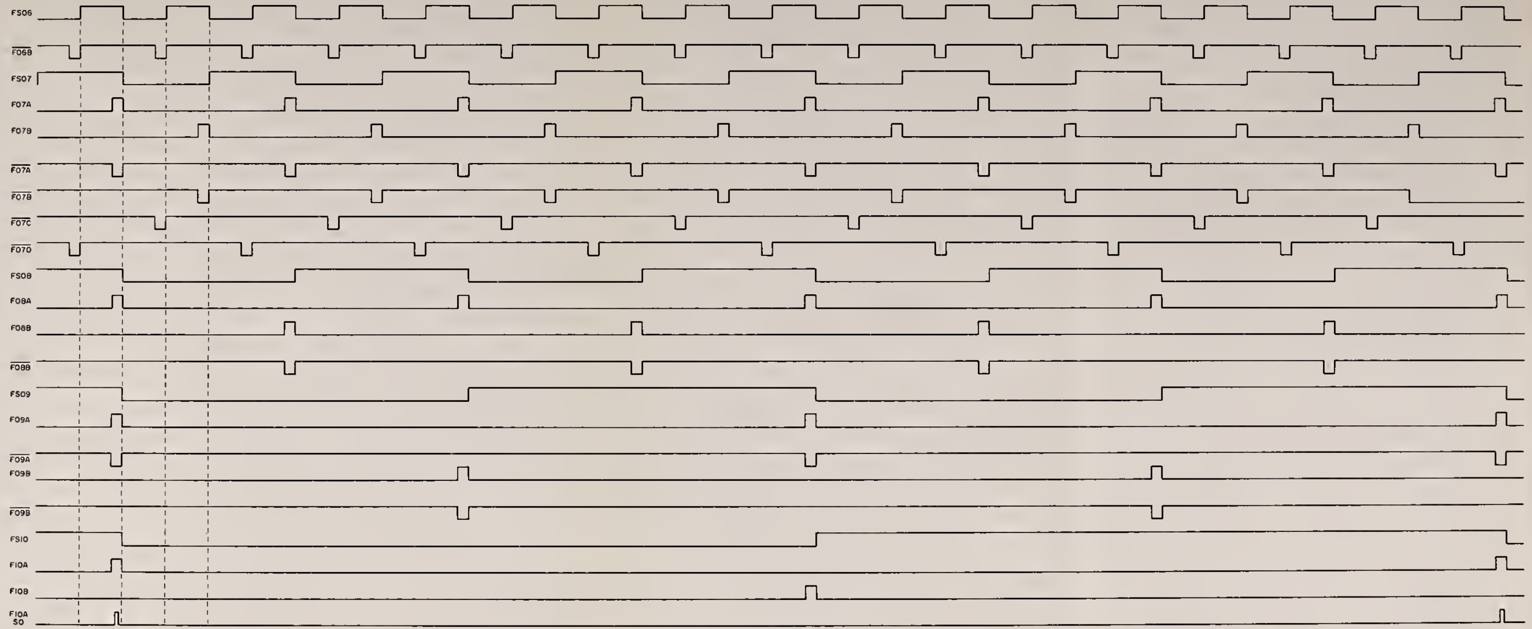

Figure 4-121. Scaler Waveforms
(Sheet 3 of 3)

The outputs from stages 1 through 17, at rates from 51.2 kpps to 0.78125 pps, are primarily used to derive timing, synchronization, and gating signals for the LGC and other systems. Table 4-VIII lists the frequency, period, and polarity of the outputs of these stages.

The output of stages 6 through 33 provides an indication of real time in the form of two 14 bit words addressable as two channels that are similar to the channels of the input-output section of the LGC. Stages 6 through 19 provide the 14 bit word to the low order channel CHAT01 through CHAT14, while stages 20 through 33 provide the 14 bit word to the high order channel CHBT01 through CHBT14. The two channels together indicate time intervals up to 23.3 hours, in 624 microsecond increments. Both words are formed by the flip-flop outputs of the respective stages, gated by a read channel signal ($\overline{\text{RCHAT}}$ or $\overline{\text{RCHBT}}$). Read signal $\overline{\text{RCHAT}}$, generated under program control as a function of octal address 0004, causes the low order bits (stages 6 through 19) to be placed on the write lines in the central processor; read signal $\overline{\text{RCHBT}}$, generated under program control as a function of address 0003, causes the high order bits (stages 20 through 33) to be placed on the write lines.

4-5.3.5 Time Pulse Generator Detailed Description. The time pulse generator, consisting of twelve flip-flop circuits, generates timing pulse outputs $\overline{\text{T01}}$ through $\overline{\text{T12}}$. This sequence of pulse outputs defines one MCT within the computer and occupies an interval of exactly 11.97 microseconds, or approximately 12 microseconds. Within this interval, access to memory and word flow take place within the computer.

Each of the timing pulses is generated by an associated flip-flop circuit shown in figure 4-122. The odd numbered outputs ($\overline{\text{T01}}$, etc.) are gated by signal $\overline{\text{ODDSET}}$ from the clock divider logic; the even numbered outputs ($\overline{\text{T02}}$, etc.) are gated by signal $\overline{\text{EVNSET}}$. Only one pulse output occurs at one time. Consider an initial condition in which signal T12 SET is generated. This signal occurs after timing pulses $\overline{\text{T01}}$ through $\overline{\text{T11}}$ have all been generated. The set output of flip-flops $\overline{\text{T01}}$ through $\overline{\text{T11}}$ are ORed through gates 37355, 37356, 37357, and 37358. When all these inputs are ZERO, output T12 SET is a ONE (coincident with $\overline{\text{EVNSET}}$) and sets the T12 flip-flop (FF37302-37303). The flip-flop reset output is gated by signal $\overline{\text{EVNSET}}$ generating signals T12 and $\overline{\text{T12}}$. Signal MT12 is made available to the CTS when this unit monitors the LGC during tests. When signal $\overline{\text{ODDSET}}$ occurs (0.97 microsecond later), the T01 flip-flop (FF37305-37306) is set by the output of gate 37304. As this flip-flop sets, the output is fed back to reset the T12 flip-flop. Simultaneously, signal $\overline{\text{ODDSET}}$ gates the flip-flop reset output generating signals T01 and $\overline{\text{T01}}$. Signal $\overline{\text{EVNSET}}$ occurs 0.97 microsecond after $\overline{\text{ODDSET}}$ and the T02 flip-flop sets, which in turn resets the T01 flip-flop.

The remaining timing pulses are generated in this manner except for the T12 output. Since T12 is generated as a function of the T12 SET signal, there is no feedback from the T12 flip-flop to reset the T11 flip-flop. The T11 flip-flop is set when output $\overline{\text{T10}}$ and $\overline{\text{ODDSET}}$ are coincident, and reset when signal $\overline{\text{EVNSET}}$ is coincident with the set output (now logic ZERO) of the T10 flip-flop.

Table 4-VIII. Scaler Outputs (Stages 1-17)

Output	Frequency	Period	Pulse Polarity
FS01, $\overline{\text{FS01}}$ F01A, F01B, F01C, F01D	51.2 kpps	19.5 μsec.	- Positive
FS02, FS02A F02A, F02B	25.6 kpps	39.0 μsec.	- Positive
FS03, FS03A F03A, F03B $\overline{\text{F03B}}$	12.8 kpps	78.0 μsec.	- Positive Negative
FS04, FS04A F04A, F04B $\overline{\text{F04B}}$	6.4 kpps	156 μsec.	- Positive Negative
FS05, $\overline{\text{FS05}}$, FS05A F05A, F05B, F05D $\overline{\text{F05A}}$, $\overline{\text{F05B}}$	3.2 kpps	312 μsec.	- Positive Negative
FS06, $\overline{\text{FS06}}$ F06A, F06B $\overline{\text{F06B}}$	1.6 kpps	624 μsec.	- Positive Negative
FS07, $\overline{\text{FS07}}$, FS07A F07A, F07B $\overline{\text{F07A}}$, $\overline{\text{F07B}}$, $\overline{\text{F07C}}$, $\overline{\text{F07D}}$	800 pps	1.25 msec.	- Positive Negative
FS08, $\overline{\text{FS08}}$ F08A, F08B $\overline{\text{F08B}}$	400 pps	2.5 msec.	- Positive Negative

(Sheet 1 of 2)

Table 4-VIII. Scaler Outputs (Stages 1-17)

Output	Frequency	Period	Pulse Polarity
FS09, $\overline{\text{FS09}}$ F09A, F09B, F09D $\overline{\text{F09A}}$, $\overline{\text{F09B}}$	200 pps	5.0 msec.	- Positive Negative
FS10 F10A, F10B $\overline{\text{F10A}}$, $\overline{\text{F10B}}$	100 pps	10 msec.	- Positive Negative
FS11 F11A, F11B	50 pps	20.0 msec.	- Positive
FS12 F12A, F12B	25 pps	40.0 msec.	- Positive
FS13 F13A, F13B	12.5 pps	80.0 msec.	- Positive
FS14 F14A, F14B	6.25 pps	160 msec.	- Positive
FS15 F15A, F15B	3.125 pps	320 msec.	- Positive
FS16 F16A, F16B	1.5625 pps	640 msec.	- Positive
FS17 F17A, F17B $\overline{\text{F17A}}$, $\overline{\text{F17B}}$	0.78125 pps	1.3 sec.	- Positive Negative

NOTE: All pulse outputs (F01A, F01B etc.) are 10 μ sec, wide regardless of frequency.

(Sheet 2 of 2)

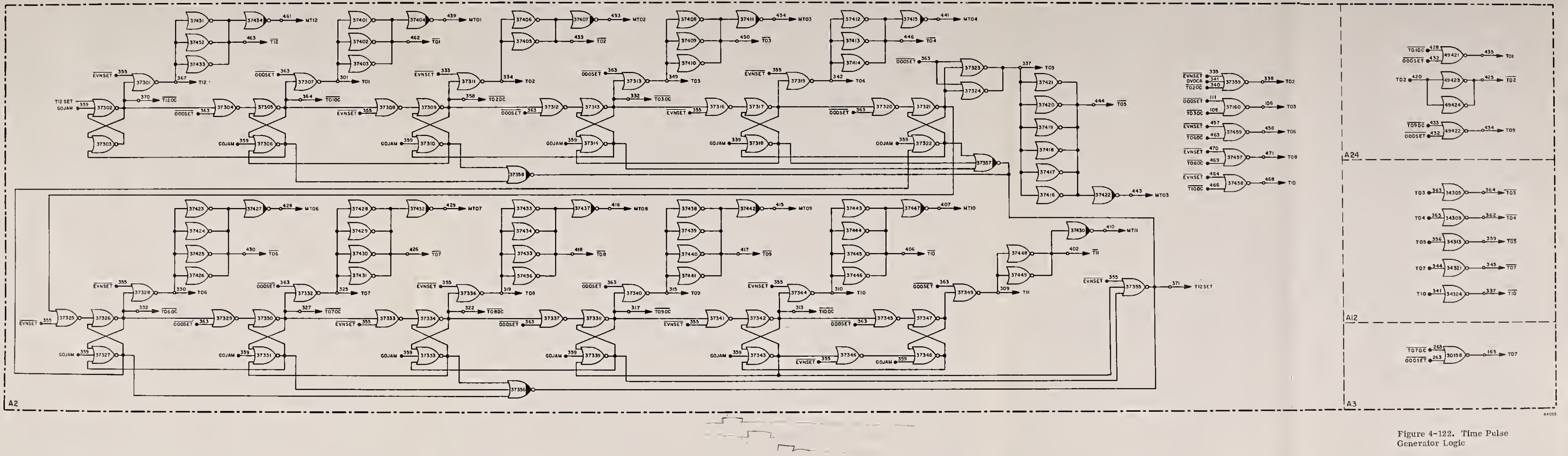

Figure 4-122. Time Pulse Generator Logic

The waveforms for the time pulse generator are shown in figure 4-123. Inputs $\overline{\text{ODDSET}}$ and $\overline{\text{EVNSET}}$ each occur at a 512 kpps rate, but are 90 degrees out of phase with each other. Consequently, even though the driving inputs are 0.75 microsecond wide, the effective drive rate of both inputs combined is twice the rate of the input. The period between each $\overline{\text{ODDSET}}$ and $\overline{\text{EVNSET}}$ pulse is 0.97 microsecond. However, time pulse outputs $\overline{\text{T01}}$ through $\overline{\text{T12}}$ are 0.75 microsecond wide.

Signal GOJAM forces the time pulse generator to indicate T12 time by resetting the T1 through T11 flip-flops, and setting the T12 flip-flop. Forcing the time pulse generator in this manner enables the cycling to be restarted beginning with T01, after a condition occurs which initiated GOJAM.

Additional drive for several of the timing pulse outputs is provided by gates located on modules A2, A3, A12, and A24. These gates are illustrated in figure 4-122. Tbe outputs (for example, T01 from gate 49421 on A24, T02 from gate 37359 on A2, etc.) are in parallel with the outputs developed by the flip-flops on module A2.

4-5.3.6 Sync and Timing Logic. The sync and timing logic, figure 4-124, generates synchronization, timing, and gating pulses for use within the computer subsystems, and synchronization pulses for systems external to the computer. These signals are developed as a function of the ring counter, strobe pulse generator, and scaler outputs.

The synchronization outputs to the external systems as well as the oscillator, clock divider logic, and the scaler outputs are generated both during normal operation and during standby. The gates on modules A1, A2, and A24 are controlled so that the supply voltage is uninterrupted when the computer is switched to standby operation. The sync and timing logic output waveforms are illustrated in figure 4-124A.

4-5.4 SEQUENCE GENERATOR. The sequence generator contains the order code processor, command generator, and control pulse generator. The sequence generator executes the instructions stored in memory by producing control pulses which regulate the data flow of the computer. The manner in which the data flow is regulated among the various functional areas of the computer and between the elements of the central processor causes the data to be processed according to the specifications of each machine instruction.

The order code processor receives signals from the central processor, priority control, and peripheral equipment. The order code signals are stored in the order code processor and converted to coded signals for the command generator. The command generator decodes these signals and produces instruction commands. The instruction commands are sent to the control pulse generator to produce a particular sequence of control pulses depending on the instruction being executed. At the completion of each instruction, new order code signals are sent to the order code processor to continue the execution of the program.

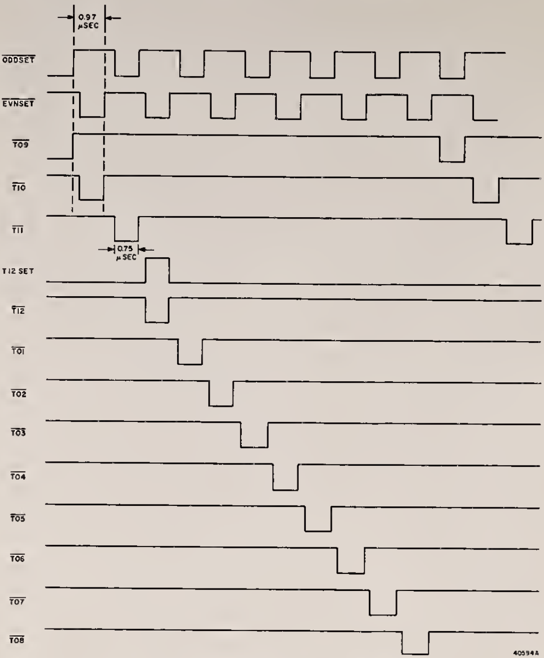

Figure 4-123. Time Pulse Generator Waveforms

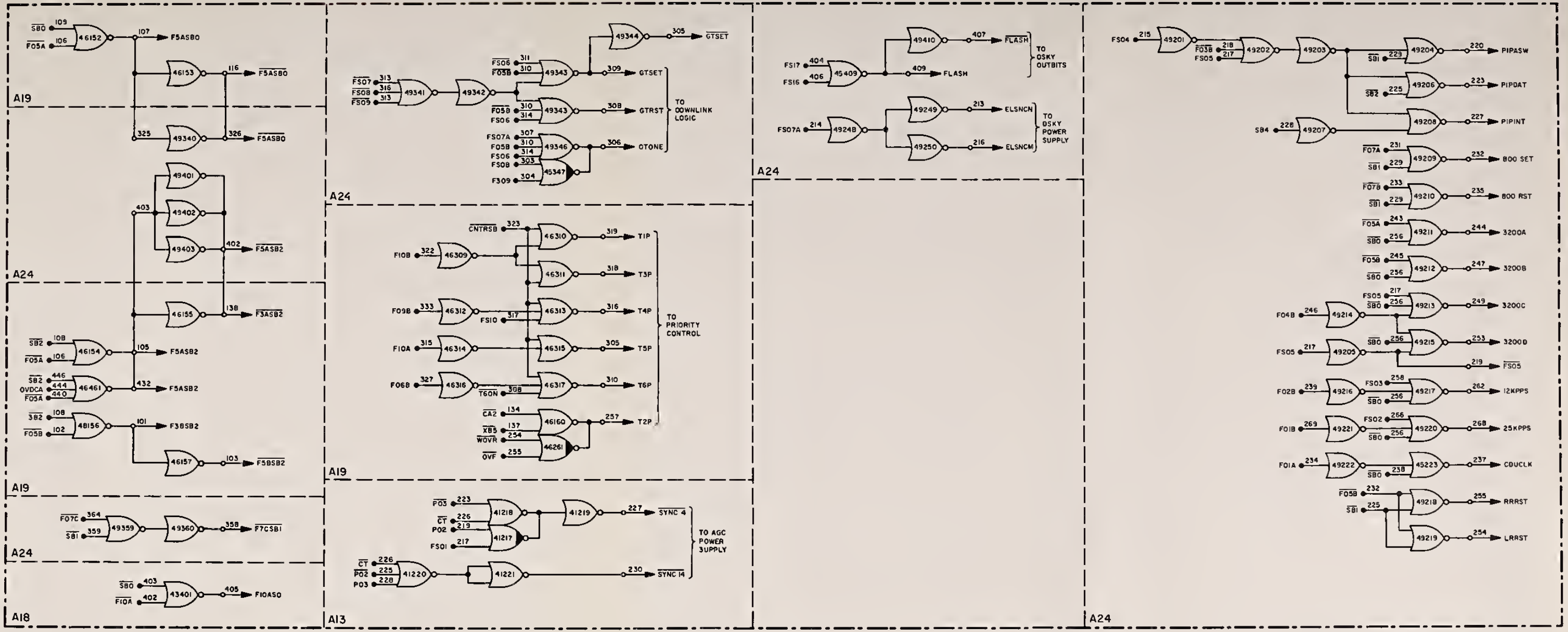

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Figure 4-124. Sync and Timing Logic

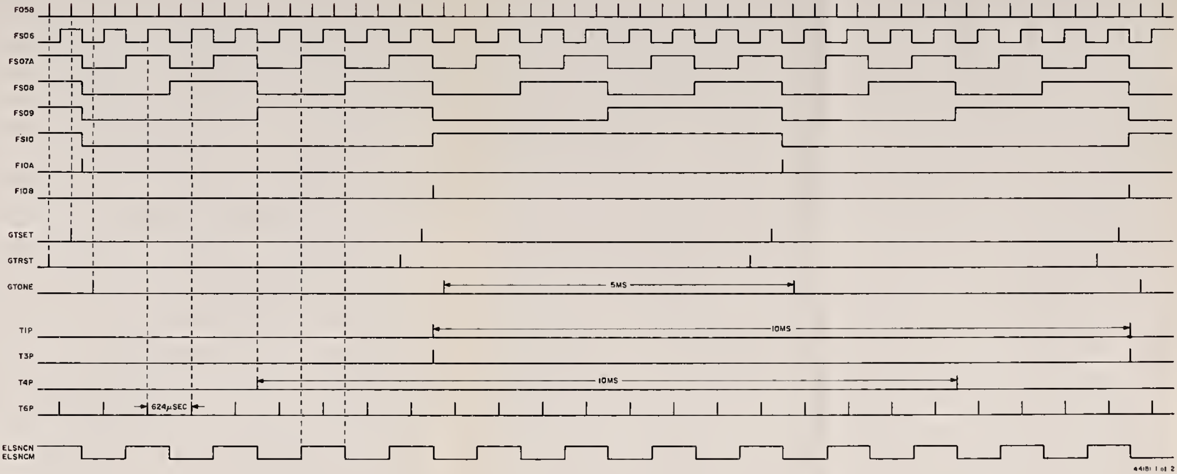


Figure 4-124A. Sync and Timing Logic Waveforms (Sheet 1 of 2)

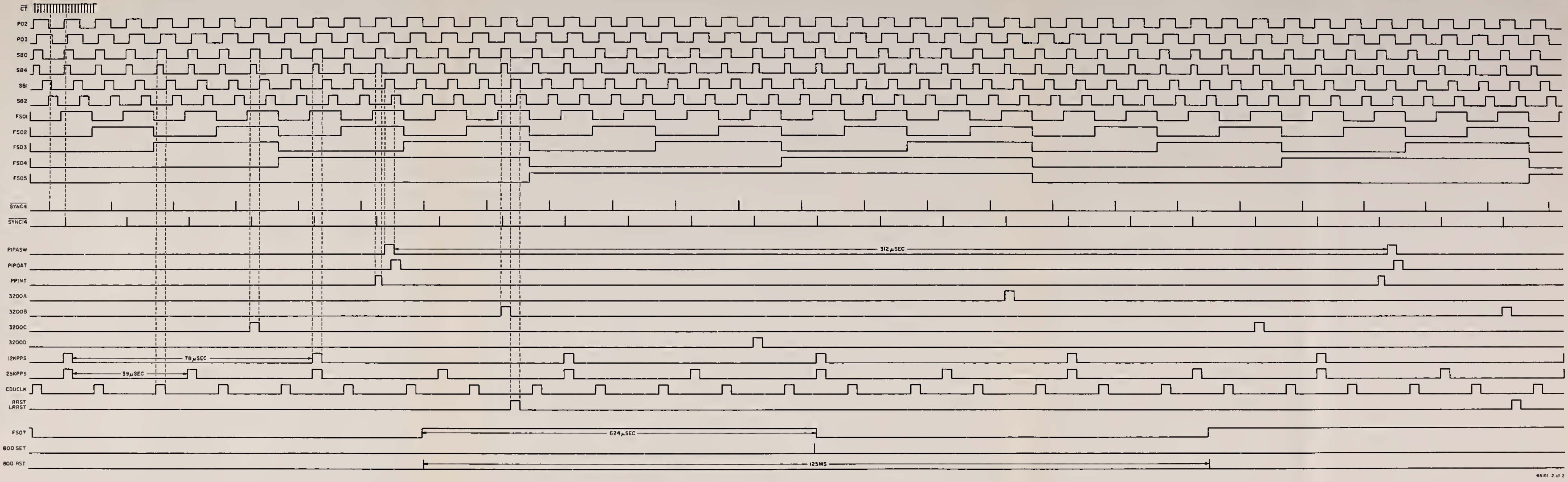


Figure 4-124A. Sync and Timing Logic Waveforms (Sheet 2 of 2)

4-5.4.1 Order Code Processor. The order code processor (figure 4-125) consists of the register SQ control, register SQ and decoders, and stage counter and decoders. The register SQ control is regulated by special purpose control pulse NISQ from the control pulse generator. Control pulse NISQ produces clear and write signals for register SQ and initiates a read signal for register B. The clear, read, and write signals place the order code content of register B onto the write lines and into register SQ. The order code signals from the priority control and the peripheral equipment pertain to start, interrupt, and transfer control to specified address instructions. These order code signals cause the register SQ control to produce the clear signal. If the order code signal is start or transfer control to specified address, no further action occurs because the order code for each of these instructions is binary 0 000 000. If the order code signal is interrupt, register SQ is set to 1 000 111. Other special purpose control pulses provide regulatory functions within the register SQ control during interrupt and some address-dependent instructions.

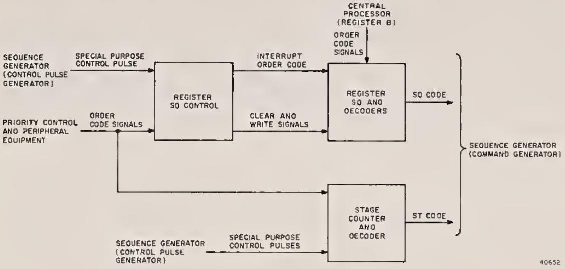

CENTRAL PROCESSOR (REGISTER B)
ORDER CODE SIGNALS
SEQUENCE GENERATOR (CONTROL PULSE GENERATOR)
SPECIAL PURPOSE CONTROL PULSE
REGISTER SQ CONTROL
INTERRUPT ORDER CODE
REGISTER SQ AND DECODERS
SQ CODE
PRIORITY CONTROL AND PERIPHERAL EQUIPMENT
ORDER CODE SIGNALS
CLEAR AND WRITE SIGNALS
SEQUENCE GENERATOR (COMMAND GENERATOR)
STAGE COUNTER AND DECODER
ST CODE
SEQUENCE GENERATOR (CONTROL PULSE GENERATOR)
SPECIAL PURPOSE CONTROL PULSES
40652

Figure 4-125. Order Code Processor, Block Diagram

Register SQ is a seven-bit register with only six of its bit positions (16 and 14 through 10) connected to the central processor write lines. The seventh (high-order) bit position is the extend bit. This high-order bit position is used for extending the order code field; it contains a logic ZERO for basic instructions and a logic ONE for extracode, channel, and interrupt instructions. Bit positions 16, 14, and 13 produce the SQ signals. At any time, only one of the eight possible SQ signals is present to indicate the octal number specified by these bit positions. Bit positions 12 and 11 contain the quarter code. These bits are decoded into one of four QC signals to indicate the octal number specified by these two bit positions. Bit position 10 is not used for basic and extracode instructions; however, it is used for the channel and interrupt instructions.

The stage counter is a three-stage Gray counter especially adapted for various counts other than the Gray code. Most instructions are several MCT's long and use the two low-order bits of the stage counter. The stage counter controls the length of each instruction. The stage counter always starts an instruction with count 000. Then it may be advanced to 001, 010, or 011 by special purpose control pulses ST1 and ST2 from the control pulse generator. The Gray code count is used for the divide instruction. Control pulse DVST advances the counter through the states 000, 001, 011, 111, 110, and 100. Then control pulse ST2 sets the stage counter to 010 to complete the divide instruction. The content of the stage counter is decoded into the ST code signals. Some of the ST code signals reflect the standard binary count from octal 0 through 3, and others reflect the Gray code count of octal 0, 1, 3, 7, 6, and 4. The order code signals from the priority control and the peripheral equipment set the stage counter to a particular state in a manner similar to that in which register SQ is set. The interrupt order code signal sets the stage counter to 000, the start order code signal sets it to 001, and the transfer control to specified address signal sets it to 011. The outputs of register SQ and stage decoders are sent to the command generator where they are used to produce subinstruction and instruction commands.

4-5.4.2 Command Generator. The command generator (figure 4-126) contains the subinstruction decoder, instruction decoder, and the counter and peripheral instruction control. The subinstruction decoder receives the SQ and ST code signals from the order code processor. These signals represent the order codes of all machine instructions and are decoded into subinstruction and instruction commands. For example, channel instruction WOR has a binary order code 1 000 101 and stage code 000. The SQ code signals SQEXT, SQ0, QC2, and SQR10 are combined with ST code signal ST0 to produce subinstruction command WOR0.

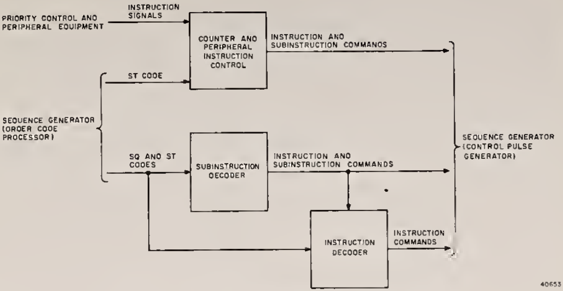

PRIORITY CONTROL AND PERIPHERAL EQUIPMENT
INSTRUCTION SIGNALS
COUNTER AND PERIPHERAL INSTRUCTION CONTROL
INSTRUCTION AND SUBINSTRUCTION COMMANDS
ST CODE
SEQUENCE GENERATOR (ORDER CODE PROCESSOR)
SQ AND ST CODES
SUBINSTRUCTION DECODER
INSTRUCTION AND SUBINSTRUCTION COMMANDS
SEQUENCE GENERATOR (CONTROL PULSE GENERATOR)
INSTRUCTION DECODER
INSTRUCTION COMMANDS
40653

Figure 4-126. Command Generator, Block Diagram

The instruction decoder receives the coded signals from the order code processor in addition to certain subinstruction commands. It produces signals called instruction commands. An instruction command is used for two or more subinstructions as compared to a subinstruction command which is used for only one subinstruction. For example, instruction command IC1 generates a combination of control pulses shared by subinstructions NDX0 and NDXX0. Instruction command IC1 is produced by signals SQEXT, SQ5, and ST0 for subinstruction NDX0 or by signals SQ5, QC0, and ST0 for subinstruction NDXX0. Other instruction commands are produced from subinstruction commands. For example, IC8 is produced by ORing DXCH0 with LXCH0.

The counter and peripheral instruction control receives instruction signals from the priority control and the peripheral equipment. These signals are applied to separate circuits which control the individual counter and peripheral instructions. The instruction signals from the priority control pertain to counter locations and the instruction(s) associated with each location. For example, signal C31A is interpreted as counter 31 address. The content of this location can only be changed by instruction DINC whose subinstruction command is produced by the counter and peripheral instruction control. Another example is signal C42P, interpreted as counter 42 positive increment or signal

C42M, counter 42 negative increment. The peripheral equipment supplies instruction signals such as MREAD and MLOAD for the fetch and store instructions, respectively. While the particular instruction is being executed, the counter and peripheral instruction control stores the input signals in the same way that order code signals are stored by register SQ. Since some of the peripheral instructions are several MCT's long, they use the ST code signals. The subinstruction and instruction command outputs of the command generator are used by the control pulse generator in conjunction with time pulses T01 through T12 to produce action pulses.

4-5.4.3 Control Pulse Generator. The control pulse generator (figure 4-127) contains the crosspoint generator, control pulse gates, and branch control. The crosspoint generator receives instruction and subinstruction commands from the command generator and branch commands from the branch control. The crosspoint generator produces an action pulse when a command signal and a time pulse are ANDed. This action is called the crosspoint operation. For example, action pulse 5XP12 is produced from subinstruction command DAS0 and time pulse T05. Many instructions use identical action pulses. When this is the case, several command signals such as TC0, TCF0, or IC4 will produce the same action pulse during time period T01. The branch commands are used to change the action pulse that normally is produced at a given time. For example, when certain conditions exist, a branch command will produce action pulse 8XP6 in addition to another action pulse normally produced at time period T08. The action pulses are supplied to the control pulse gates which convert them to specific control pulses for use in instruction execution.

The control pulse gates perform the Boolean NOR function. There is one gate for each control pulse. These gates split the action pulses into as many control pulses as

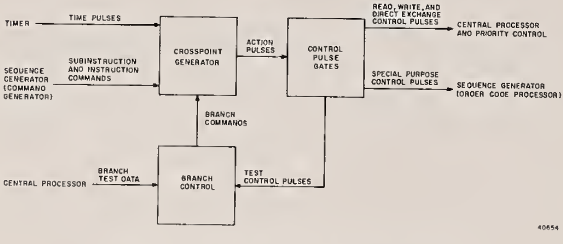

TIMER
TIME PULSES
SEQUENCE GENERATOR (COMMAND GENERATOR)
SUBINSTRUCTION AND INSTRUCTION COMMANDS
CROSSPOINT GENERATOR
ACTION PULSES
CONTROL PULSE GATES
READ, WRITE, AND DIRECT EXCHANGE CONTROL PULSES
CENTRAL PROCESSOR AND PRIORITY CONTROL
SPECIAL PURPOSE CONTROL PULSES
SEQUENCE GENERATOR (ORDER CODE PROCESSOR)
BRANCH COMMANDS
CENTRAL PROCESSOR
BRANCH TEST DATA
BRANCH CONTROL
TEST CONTROL PULSES
40654

Figure 4-127. Control Pulse Generator, Block Diagram

are required for a particular operation. For example, action pulse 3XP6 is converted to control pulses RZ and WQ. Some of the control pulses produced by the control pulse gates are used by the sequence generator. These include the special purpose control pulses which control the operation of the order code processor and the test control pulses which are applied to the branch control. The other control pulse groups, namely the read, write, and direct exchange control pulses are used in the central processor and the priority control. The purpose of each control pulse is described in paragraph 4-5.2, Machine Instructions.

The branch control is connected to the write lines of the central processor. Data which is placed onto the write lines by read control pulses is tested in the branch control. The branch control contains two stages. Branch 1 normally tests for sign and branch 2 tests for full quantities such as plus or minus zero. Both branches test for positive and negative overflow and have the overflow bits written directly into the branch register. Positive overflow is 01 where branch 1 is the high order bit. Negative overflow is 10. The branch commands sent to the crosspoint generator affect the action pulses at given times. The branch control also contains the special instruction flip-flop which controls the execution of RELINT, INHINT, and EXTEND instructions.

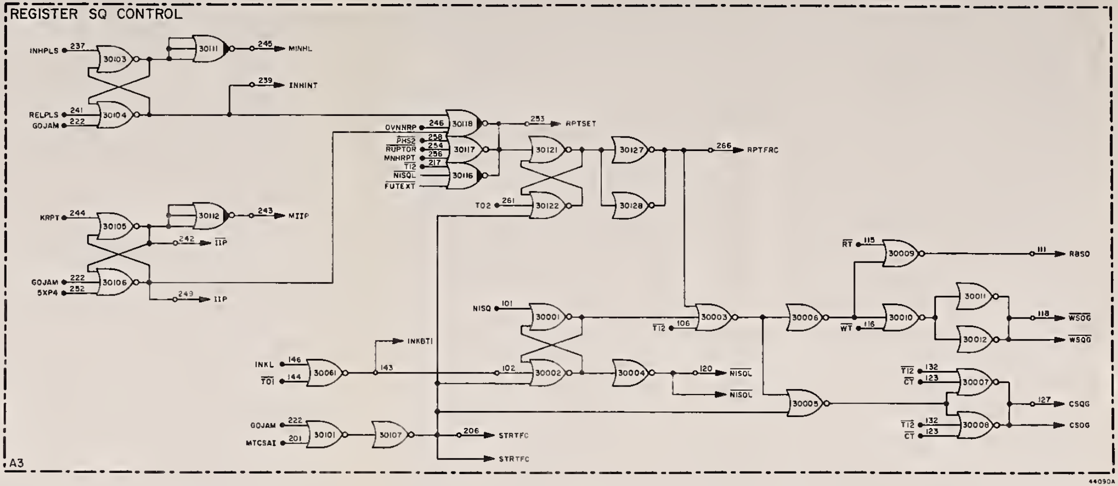
4-5.4.4 Register SQ Control. The register SQ control (figure 4-128) is regulated by special purpose control pulse NISQ from the control pulse generator. Control pulse NISQ causes the register SQ control to produce clear signal CSQG, read signal RBSQ, and write signal WSQG. These signals place the order code (content of register B) onto the write lines and into register SQ at the beginning of each new instruction. The order code signals applied to the register SQ control from the priority control (GOJAM and RUPTOR) and peripheral equipment (MTCSAI) pertain to start, interrupt, and transfer control to specified address instructions, respectively. A distinct priority is associated with each of these three instructions. Interrupt and transfer control to specified address instructions can never be requested when the computer is forcing the execution of the start instruction, which has the highest priority. Certain peripheral instructions occupy the next level of priority, followed by the counter instructions and in turn the transfer control to specified address instruction, which has priority over the interrupt instruction; all six of these instruction categories have priority over basic instructions. In addition, the interrupt instruction cannot be executed when the next instruction being called is an extracode instruction. The register SQ control establishes this priority. It also provides signals to force register SQ to the 0 000 000 state for start and transfer control to specified address instructions, and state 1 000 111 for the interrupt instruction. The register SQ control is able to inhibit the processing of all subsequent interrupts when specified by the program and will permit only one interrupt to be processed at a time. Certain monitor functions built into the register SQ control may be used when the computer is connected to the peripheral equipment.

When control pulse NISQ is applied to the set side of the NISQL flip-flop (figure 4-128), the NISQL flip-flop will set, provided signal STRTFC is not present. Control pulse NISQ is produced during time period T02 or T08 depending on the subinstruction which produces the control pulse. Once the NISQL flip-flop is set, it remains set until signal INKBT1 or STRTFC is produced. Signal INKBT1 occurs at time period T01 when no counter incrementing is in progress as indicated by the absence of signal INKL. Signal STRTFC may occur anytime during an MCT if produced by signal GOJAM or at a time period predetermined by the peripheral equipment if produced by signal MTCSAI.

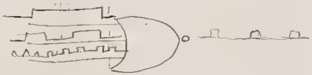
Signals CSQG, RBSQ, and WSQG are produced during time period T12 provided that the NISQL flip-flop is set and signal RPTFRC is not present. The clear, read, and write signals are phased by the clear timing signal CT, the read timing signal RT, and the write timing signal WT, respectively. When the start or transfer control to specified address instruction is to be executed, the NISQL flip-flop is reset and signals RBSQ and WSQG are inhibited. However, signal CSQG is produced by signal STRTFC and forces the SQ register to the 0 000 000 state. If signal RPTFRC is present, signals CSQG, RBSQ, and WSQG are not produced. Signal RPTFRC is applied to register SQ and forces it to the 1 000 111 state.

The priority control supplies signal RUPTOR to the register SQ control when the interrupt instruction is to be executed. Signal RUPTOR may be inhibited in the register SQ control by several conditions, one of which is the programmed interrupt inhibit called INHINT. The INHINT condition is established by executing instruction INHINT whose order code is 00.0004. This instruction produces signal INHPLS which is applied to the set side of the INHINT flip-flop (figure 4-128). The INHINT flip-flop will set provided signal GOJAM is not present at the application of signal INHPLS. Once the flip-flop is set, it remains set until signal GOJAM or RELPLS is produced. Signal RELPLS is produced by instruction RELINT which releases the interrupt inhibit condition. Instruction RELINT has the order code 00.0003. Signal MINHL from the INHINT flip-flop is connected to an indicator on the peripheral equipment. This indicator lights when the INHINT flip-flop is set.

Another condition which inhibits signal RUPTOR is the interrupt in progress (IIP) condition. The IIP condition is established during the execution of the interrupt instruction to indicate that an interrupt is in progress. Subinstruction RUPT0 produces signal KRPT which is applied to the set side of the IIP flip-flop (figure 4-128). The IIP flip-flop will set, provided signal GOJAM is not present at the application of signal KRPT. Signal KRPT is an action or crosspoint pulse (9XP1) produced during time period T09 of subinstruction RUPT0. Once the IIP flip-flop is set, it remains set until signal GOJAM or 5XP4 is produced. Signal 5XP4 is produced by subinstruction RSM3 which is executed at the completion of an interrupt sequence. Subinstruction RSM3 is part of the RESUME instruction (order code 05.0017) which returns control to the program that was being executed before the interrupt occurred. Signal 5XP4 is also an action or crosspoint pulse which is produced during time period T05. Signal MIIP from the IIP flip-flop is connected to the peripheral equipment. A switch on the peripheral equipment will permit signal MIIP to light an indicator and to cause a monitor T12 stop. This causes the time pulse generator (which produces signals T01 through T12) to stop at time period T12 until it is released by the peripheral equipment. The peripheral equipment can supply signal MNHRPT to the register SQ control. This signal is produced by a switch closure and inhibits signal RUPTOR. Signal OVNHRP inhibits signal RUPTOR for all multiply subinstructions preceding MP3 while the accumulator is being used in double-precision operations.



REGISTER SQ CONTROL	
SIGNAL	EQUATION
NISQL	NISQ $\overline{STRTFC}$ + INKBT1 $\overline{STRTFC}$ NISQL
INKBT1	$\overline{INKL}$ T01
STRTFC	GOJAM + MTCSAI
CSQG	(NISQL $\overline{RPTFRC}$ + STRTFC) T12 CT
RBSQ	NISQL $\overline{RPTFRC}$ T12 RT
WSQG	NISQL $\overline{RPTFRC}$ T12 WT
INHINT	INHPLS $\overline{GOJAM}$ + INHINT $\overline{RELPLS}$ $\overline{GOJAM}$
IIP	KRPT $\overline{GOJAM}$ + IIP $\overline{5XP4}$ $\overline{GOJAM}$
RPTFRC	RUPTOR NISQL T12 PHS2 $\overline{INHINT}$ $\overline{IIP}$ $\overline{MNHRPT}$ $\overline{FUTEXT}$ $\overline{STRTFC}$ + STRTFC $\overline{T02}$ RPTFRC



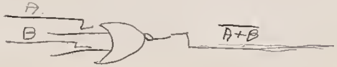


Figure 4-128. Register SQ Control, Logic Diagram

Signal FUTEXT is produced by the register SQ and decoder circuits. This signal is present when the next instruction to be executed is an extracode instruction. Signal FUTEXT is produced when instruction EXTEND or NDX is executed and occurs at time period T08 or T10, respectively. Signal RUPTOR is inhibited by the future extend condition because this condition cannot be re-established when returning to the interrupted program through instruction RESUME. The order codes for instructions EXTEND and NDX which establish the future extend condition are 00. 0006 and 15, respectively.

Signal RUPTOR will cause the RPTFRC flip-flop to set at time period T12 subject to the phasing of signal PHS2. A new instruction must be in the process of being called in order for the RPTFRC flip-flop to set. This condition is established by signal NISQL. The RPTFRC flip-flop will set only if signal STRTFC is not present at the same time the set signal is present. The flip-flop is reset at time period T02 or when signal GOJAM or MTCSAI is present.

4-5.4.5 Register SQ and Decoders. Register SQ is a seven-bit register which stores the content of the extended order code field as each instruction is being executed. The content of register SQ and decoders produces signals SQEXT, SQ0 through SQ7, QC0 through QC3, and SQR10. These signals are used by the command generator to produce subinstruction and instruction commands.

Register SQ (figure 4-129) is connected to the central processor by write line signals WL16 and WL14 through WL10. The register SQ control produces signal RBSQ which places the order code content of register B onto the write lines. It also produces signal CSQG which clears register SQ and WSQG which writes the new order code into register SQ. Signal CSQG does not clear the SQEXT bit position. This bit position is set when an extracode instruction is to be exccuted and is controlled by the FUTEXT flip-flop.

Special purpose control pulses EXTPLS and EXT are applied to the set side of the FUTEXT flip-flop. The flip-flop will set provided signal STRTFC is not present at the application of signals EXTPLS or EXT. Signal EXTPLS is produced at time pulse T08 by instruction EXTEND. The order code for the EXTEND instruction is 00. 0006. Signal EXT is produced at time pulse T10 of subinstruction NDXX1. The FUTEXT flip-flop remains set until signal INKBT1 or STRTFC is produced. Signal INKBT1 occurs at time pulse T01 when no counter incrementing is in progress.

The SQEXT flip-flop can be set at time pulse T12 provided the NISQL and the FUTEXT flip-flops are set. If signal STRTFC is present, the NISQL and FUTEXT flip-flops will be reset and their outputs will cause the SQEXT flip-flop to reset also. Signal RPTFRC also sets the SQEXT flip-flop provided a new instruction is being called and signal STRTFC is not present. Once the SQEXT flip-flop is set, it remains set until the next basic instruction is executed. The resetting of the SQEXT flip-flop is accomplished when signal FUTEXT is not present and signals NISQL and T12 are.

When the start or transfer control to specified address instruction is to be executed, signal STRTFC resets the SQEXT flip-flop as specified in the preceeding paragraph. It also produces signal CSQG which clears bit positions 16 and 14 through 10 of register SQ. As a result, register SQ is forced to the 0 000 000 state which causes the execution of instruction GOJ or TCSA depending on the state of the stage counter. When the interrupt instruction is to be executed, signal RPTFRC sets bit positions SQEXT and 12 through 10 and resets bit positions 10, 14, and 13 of register SQ. As a result, register SQ is forced to the 1 000 111 state which causes the execution of instruction RUPT.

Signals MSQEXT, MSQ16, and MSQ14 through MSQ10 are connected to indicators on the peripheral equipment so that the content of register SQ can be monitored at any time.

The SQ decoder produces signals SQ0 through SQ7 from the outputs of bit positions 16, 14, and 13 of register SQ. These signals are used in the command generator together with signals SQEXT, QC0 through QC3, and SQR10 to produce subinstruction and instruction commands. Signals SQ0 through SQ7 are inhibited by signal INKL. Signal INKL is produced when a counter instruction is being executed. When signal INKL is present, no commands can be produced other than those for the counter and peripheral instructions.

The QC decoder produces signals QC0 and QC3 for the outputs of bit positions 12 and 11 of register SQ. These signals are also used to produce subinstruction and instruction commands and are not inhibited by counter incrementing.

4-5.4.6 Stage Counter and Decoder. The stage counter and decoder (figure 4-130) is regulated by special purpose control pulses ST1, ST2, DVST, RSTSTG, and TRSM from the control pulse generator and by order code signals GOJAM and MTCSAI from the priority control and peripheral equipment, respectively. The stage counter is used as a storage device which is forced to a different state after the execution of each subinstruction. The stage counter remains in a given state for one MCT, the duration of every subinstruction. The stage counter is forced through various counts depending on the instruction being executed. Most instructions are two MCT's long and are completed by executing subinstruction STD2. As a result, the stage counter is advanced through states 000 and 010. Some instructions are three MCT's long and are completed by executing subinstruction STD2. The stage counter states for these instructions are 000, 001, and 010. Other combinations of states are simply 000 for the transfer control instruction, 000 and 001 for the index instructions, 000 and 011 for the RESUME instruction, and 000, 001, and 011 for the multiply instruction. The divide instruction is seven MCT's long. Gray code counts 000, 001, 011, 111, 110, and 100 are used to enumerate six MCT's of this instruction. The seventh MCT is controlled by state 010 which is that of subinstruction STD2.

The stage counter contains three primary level flip-flops A, B, and C, and three secondary level flip-flops STG1, STG2, and STG3, respectively. The secondary level flip-flops are set to the state of the primary level flip-flops at time pulse T12 for most instructions. For the divide instruction, the transfer of states occurs at time pulses T03 and T12. The primary level flip-flops are reset at time pulse T01 to establish the state 000.

REGISTER SQ

SIGNAL	EQUATION
FUTEXT	$(EXTPLS + EXT)\ \overline{STRTFC} + \overline{INKBT1}\ \overline{STRTFC}\ FUTEXT$
SQEXT	$FUTEXT\ \ NISQ\ \ T12 + RPTFRC\ \ \overline{NISQL\ \ T12}\ \ \overline{STRTFC} + SQEXT\ (FUTEXT + \overline{NISQL\ \ T12}\ \ \overline{STRTFC})$
SQR16	$WL16\ \ WSQG\ \ \overline{CSQG} + SQR16\ \ \overline{CSQG}\ \ \overline{RPTFRC}$
SQR14	$WL14\ \ WSQG\ \ \overline{CSQG} + SQR14\ \ \overline{CSQG}\ \ \overline{RPTFRC}$
SQR13	$WL13\ \ WSQG\ \ \overline{CSQG} + SQR13\ \ \overline{CSQG}\ \ \overline{RPTFRC}$
SQR12	$WL12\ \ WSQG\ \ \overline{CSQG} + RPTFRC + SQR12\ \ \overline{CSQG}$
SQR11	$WL11\ \ WSQG\ \ \overline{CSQG} + RPTFRC + SQR11\ \ \overline{CSQG}$
SQR10	$WL10\ \ WSQG\ \ \overline{CSQG} + RPTFRC + SQR11\ \ \overline{CSQG}$

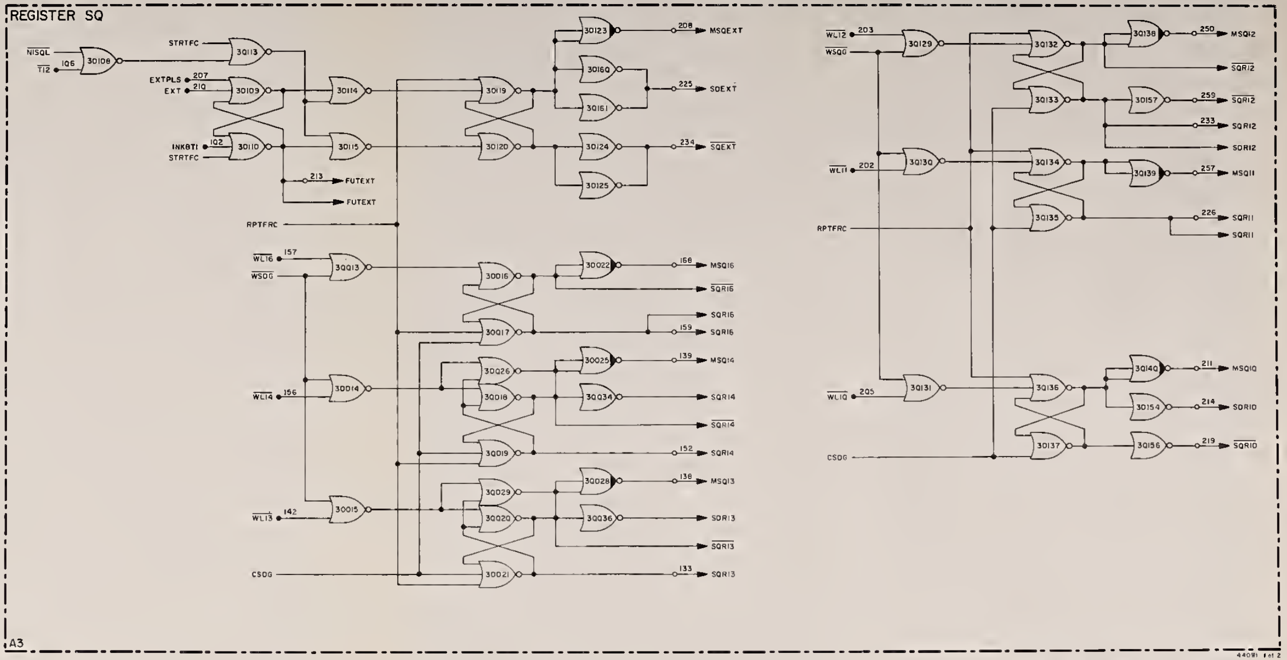
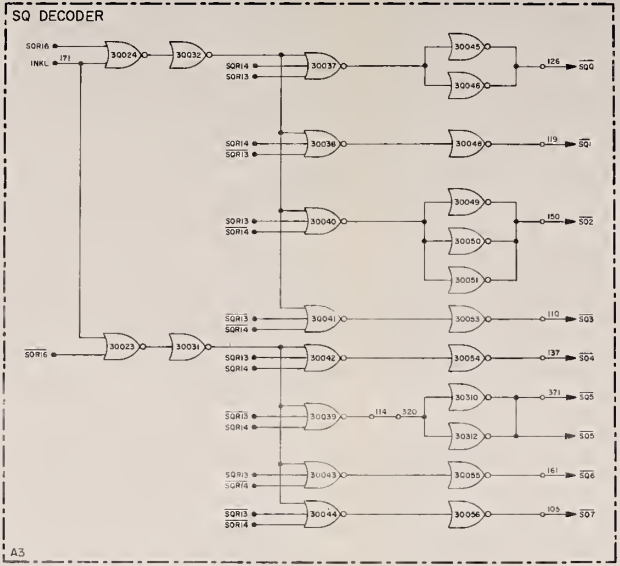
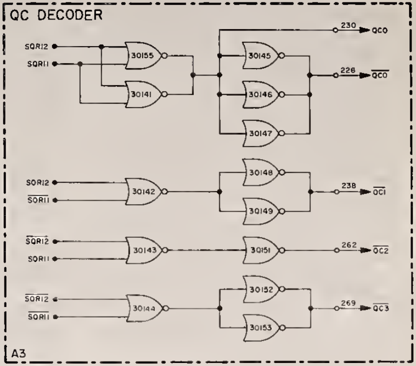


Figure 4-129. Register SQ and Decoder, Logic Diagram (Sheet 1 of 2)





SQ DECODER

SIGNAL	EQUATION
SQ0	$\overline{SQR16}$ $\overline{SQR14}$ $\overline{SQR13}$ $\overline{INKL}$
SQ1	$\overline{SQR16}$ $\overline{SQR14}$ SQR13 $\overline{INKL}$
SQ2	$\overline{SQR16}$ SQR14 $\overline{SQR13}$ $\overline{INKL}$
SQ3	$\overline{SQR16}$ SQR14 SQR13 $\overline{INKL}$
SQ4	SQR16 $\overline{SQR14}$ $\overline{SQR13}$ $\overline{INKL}$
SQ5	SQR16 $\overline{SQR14}$ SQR13 $\overline{INKL}$
SQ6	SQR16 SQR14 $\overline{SQR13}$ $\overline{INKL}$
SQ7	SQR16 SQR14 SQR13 $\overline{INKL}$

QC DECODER

SIGNAL	EQUATION
QC0	$\overline{SQR12}$ $\overline{SQR11}$
QC1	$\overline{SQR12}$ SQR11
QC2	SQR12 $\overline{SQR11}$
QC3	SQR12 SQR11

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Figure 4-129. Register SQ and Decoder, Logic Diagram (Sheet 2 of 2)

STAGE COUNTER	
SIGNAL	EQUATION
A	ST1 + (GOJAM + MTCSAI) $\overline{T01}$ + OVST $\overline{STG3}$ + A $\overline{T01}$
B	ST2 $\overline{GOJAM}$ + MTCSAI $\overline{T01}$ + OVST STG1 $\overline{GOJAM}$ + NOR100 X87 XT1 TRSM $\overline{GOJAM}$ $\overline{T01}$ + B $\overline{T01}$ GOJAM
C	OVST STG2 $\overline{STRTFC}$ + C $\overline{T01}$ $\overline{STRTFC}$ · $\overline{RSTSTG}$
T12USE	OVST $\overline{GOJAM}$ + T12USE $\overline{GOJAM}$ $\overline{RSTSTG}$
D	T12 $\overline{T12USE}$ PHS3 + T03 T12USE PHS3
STG1	A D + STG1 (A + $\overline{D}$)
STG2	B D + STG2 (B + $\overline{D}$)
STG3	C D + STG3 (C + $\overline{D}$)

STAGE DECODER	
SIGNAL	EQUATION
ST0	$\overline{STG3}$ $\overline{STG2}$ $\overline{STG1}$
ST02	$\overline{STG3}$ STG2 $\overline{STG1}$ $\overline{INKL}$
ST3	$\overline{STG3}$ STG2 STG1
ST10	$\overline{STG3}$ $\overline{STG2}$ STG1
ST1376	ST10 + ST376
ST376	STG2 (STG1 + STG3)
ST3764	ST376 + ST4
ST4	STG3 $\overline{STG2}$ $\overline{STG1}$

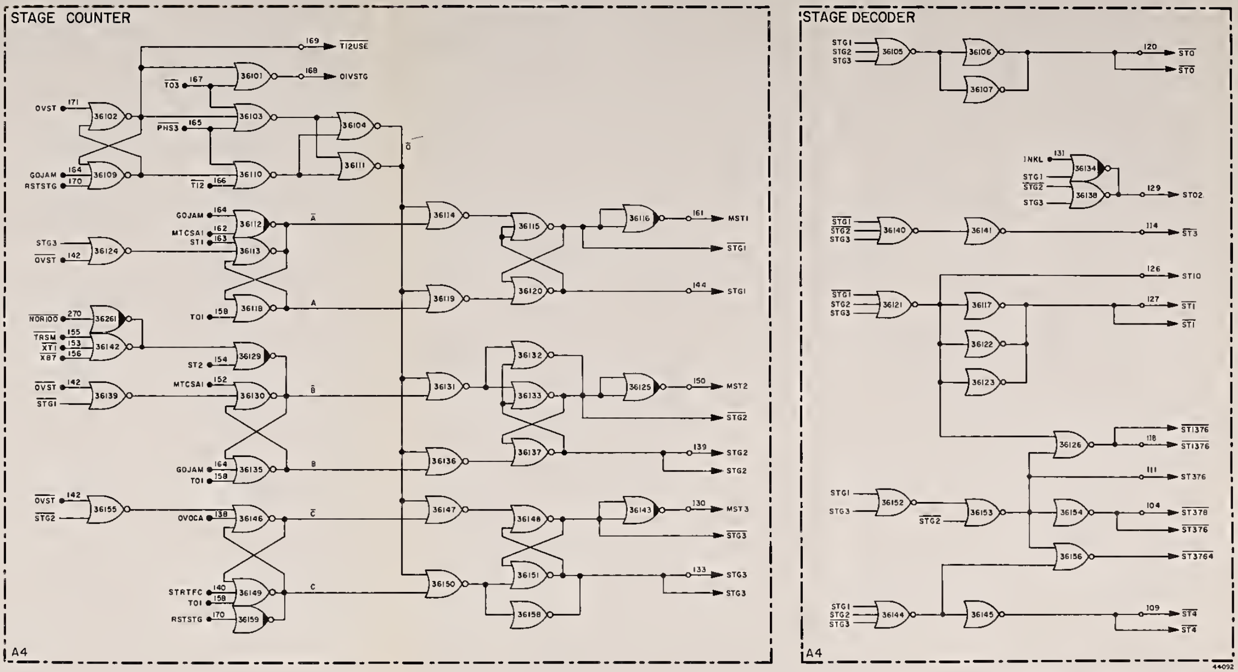

Figure 4-130. Stage Counter and Decoder, Logic Diagram

The stage counter can establish state 001 three ways. When the start instruction is to be executed, signal GOJAM sets flip-flop A and resets flip-flop B. Flip-flop C is reset by signal STRTFC. Control pulse ST1 sets flip-flop A (at time pulse T10) and control pulse DVST sets the flip-flop (at time pulse T02) provided that flip-flop STG3 is not set during the Gray code count sequence.

The state 010 can only be produced in one way, by control pulse ST2 which sets flip-flop B at time pulse T08 or T10 depending on the subinstruction which produces the control pulse.

The state 011 can be produced four ways. When the transfer control to specified address instruction is to be executed, signal MTCSAI sets flip-flops A and B and signal STRTFC resets flip-flop C. During the execution of subinstruction MP1, control pulses ST1 and ST2 are produced at time pulse T10. These control pulses set flip-flops A and B and cause the execution of subinstruction MP3. During the execution of instruction RESUME, control pulse TRSM sets flip-flop B at time pulse T05. Instruction RESUME is an address-dependent instruction consisting of subinstructions NDX0 and RSM3. The content of register S must be octal 0017 for control pulse TRSM to set flip-flop B. At time pulse T10 of subinstruction NDX0, control pulse ST1 sets flip-flop A thereby establishing the state 011 for subinstruction RSM3. During the execution of the divide instruction, control pulse DVST sets flip-flop A at time pulse T02 provided that flip-flop STG3 is not set. Flip-flop B is set by DVST provided flip-flop STG1 is set. Since flip-flop STG2 is not set when control pulse DVST is produced, flip-flop C remains reset, thus establishing state 011.

States 111, 110, and 100 are established by control pulse DVST at time pulse T02 of instruction divide. Flip-flops A, B, and C are set provided that flip-flop STG3 is not set and flip-flops STG1 and STG2 are set, respectively. This establishes state 111. States 110 and 100 are established in a similar way and are dependent on the states of flip-flops STG1, STG2, and STG3.

The contents of flip-flops A, B, and C are transferred to flip-flops STG1, STG2, and STG3, respectively, at time pulse T12 if the T12USE flip-flop is not set. The transfer is subject to the phasing of signal PHS3. The T12USE flip-flop is set at time pulse T02 by control pulse DVST provided signal GOJAM is not present. Once the flip-flop is set, it remains set until reset by control pulse RSTSTG (which occurs at time pulse T08 of subinstruction DV4) unless signal GOJAM occurs first. When the T12USE flip-flop is set, the contents of the primary level flip-flops are transferred to the secondary level flip-flops at time pulse T03 according to the phase of signal PHS3. Signal DIVSTG is also produced at time pulse T03 under these conditions. When the secondary level flip-flops are set, they cannot be reset unless signal D is present. Signals MST1, MST2, and MST3 are connected to lights on the peripheral equipment to indicate the state of the stage counter.

The stage decoder (figure 4-130) produces signals ST0, ST1D, STD2, ST3, ST4, ST1376, ST376, and ST3764. This signal group is the decoded output of the stage counter and is used in conjunction with signals SQEXT, SQ0 through SQ7, QC0 through QC3, and SQR10 to produce subinstruction and instruction commands. Signals ST0, ST1D, STD2, ST3 and ST4 are produced when the stage counter is set to states 000, 001, 010, 011, and 100, respectively. Signal ST376 is produced when the stage counter is in state 011, 111, or 110. Likewise, signal ST1376 is produced when the stage counter is set to state 001, 011, 111, or 110, and signal ST3764 is produced during states 011, 111, 110, or 100.

4-5.4.7 Subinstruction Decoder. The subinstruction decoder receives the SQ and ST code signals from the order code processors and produces signals called subinstruction and instruction commands. Signals SQEXT, SQ0 through SQ7, QC0 through QC3, and SQR10 comprise the SQ code signals. Signals ST0 through ST4, ST376, ST1376, and ST3764 comprise the ST code signals. The SQEXT and SQR10 signals represent the high and low order bits, respectively, of register SQ. Signals SQ0 through SQ7 represent octal quantities 0 through 7 respectively, in bit positions 16, 14, and 13 of register SQ. Signals QC0 through QC3 represent octal quantities 0 through 3, respectively, in bit positions 12 nnd 11 of register SQ. The SQ and QC signals are the decoded outputs of the register SQ and decoder circuits. The ST code signals represent the state of the stage counter. For example, signal ST1 represents state 001. The ST signals are the decoded outputs of the stage counter and decoder circuits.

The subinstruction decoder utilizes the SQ and ST code signals in producing subinstruction and instruction commands. The command signals in turn are ANDed with time pulses T01 through T12 as necessary to produce crosspoint signals. This action is accomplished in the crosspoint generator. The crosspoint signals produce the control pulses which regulate the data flow of the computer. By definition, a subinstruction command is used for only one subinstruction. For example, command STD2 is used only during subinstruction STD2. An instruction command is therefore defined as a command which is used by two or more subinstructions. For example, command IC3 is used for subinstructions STD2, TC0, and TCF0. Table 4-IX lists all of the commands produced by the various SQ and ST codes. The subinstructions which relate to the specific SQ and ST codes are also listed in table 4-IX.

Figure 4-131 shows the logic circuits that produce the subinstruction commands for basic, channel, and extracode instructions. Signal CCS0 is used as an example to illustrate the production of commands. When subinstruction CCS0 is to be executed, register SQ is set to the 0 001 00X state and the stage counter is set to 000. As a result, the order code processor supplies signals SQ1, QC0, and ST0 to the command generator. Since CCS is a basic instruction, the high order bit of register SQ is a logic ZERO and signal SQEXT is not present. The circuit for basic instructions detects this condition and produces signal NEXST0. Had signal ST1 been present instead of ST0, signal NEXST0 would not be produced. Signals NEXST0, SQ1, and QC0 are then ANDed to produce subinstruction command CCS0.

The QC signals are produced by the two high order bits of the address field. Instructions which do not use the extended order code field have commands that are produced

Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
BASIC INSTRUCTIONS				
STD2		2		STD2 IC3
TC0	00	0		TC0 IC3
CCS0	010	0		CCS0 IC12
TCF0	012 014 016	0		TCF0 IC3
DAS0	020	0		DAS0 IC10
DAS1	020	1		DAS1
LXCH0	022	0		IC8 IC9
INCR0	024	0		INCR0 PRINC
ADS0	026	0		ADS0 DAS1
CA0	03	0		IC6 IC13
CS0	04	0		IC7 IC13
NDX0	050	0		NDX0 IC1 IC13
NDX1	050	1		IC2
RSM3	050	3		RSM3

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Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
BASIC INSTRUCTIONS (cont)				
DXCH0	052	0		DXCH0 IC8 ICI0
DXCH1	052	1		IC5 IC9
TS0	054	0		TS0 IC9
XCH0	056	0		IC5 IC9
AD0	06	0		AD0 IC11 IC13
MASK0	07	0		MASK0 IC14
EXTRACODE INSTRUCTIONS				
DV0	I10	0		DV0 DIV
DV1	I10	1		DVI DV1376 DIV
DV3	110	3		DV1376 DV376 DIV
DV7	110	7		DVI376 DV376 DIV

(Sheet 2 of 6)

Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
EXTRACODE INSTRUCTIONS (cont)				
DV6	110	6		DV1376 DV376 DIV
DV4	110	4		DV4
BZF0	112 114 116	0	XX X0 X1	IC15 IC17 IC16
MSU0	120	0		MSU0 IC12
QXCH0	122	0		QXCH0 IC9
AUG0	122	0		AUG0 PRINC
DIM0	126	0		DIM0 PRINC
DCA0	13	0		DCA0 IC4 IC10 IC13
DCA1	13	1		IC6 IC13
DCS0	14	0		DCS0 IC4 IC10 IC13
DCS1	14	1		IC7 IC13

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Table 4-1X. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
EXTRACODE INSTRUCTIONS (cont)				
NDXX0	15	0		IC1 IC13
NDXX1	15	1		NDXX1 IC2
SU0	160	0		SU0 IC11 IC13
BZMF0	162 164 166	0	XX 00 X1 1X	IC15 IC17 IC16 IC16
MP0	17	0		MP0 IC14
MP1	17	1		MP1
MP3	17	3		MP3
CHANNEL INSTRUCTIONS				
READ0	100	0		READ0 INOUT
WRITE0	101	0		WRITE0 INOUT
RAND0	102	0		RAND0 INOUT
WAND0	103	0		WAND0 INOUT
ROR0	104	0		ROR0 INOUT

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Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
CHANNEL INSTRUCTIONS (cont)				
WOR0	105	0		WOR0 INOUT
RXOR0	106	0		RXOR0 INOUT IC14
INTERRUPT INSTRUCTIONS				
RUPT0	107	0		RUPT0
RUPT1	107	1		RUPT1
GOJ1	00	1		GOJ1
COUNTER INSTRUCTIONS				
PINC				PINC PARTC INKL
MINC				MINC PARTC INKL
PCDU				PCDU PARTC INKL
MCDU				MCDU PARTC INKL
DINC				DINC PARTC INKL
SHINC				SHIFT INKL
SHANC				SHANC SHIFT INKL

(Sheet 5 of 6)

Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
PERIPHERAL INSTRUCTIONS				
TCSAJ3	00	3		TCSAJ3
INOTRD				CHINC INKL MON+CH
INOTLD				INOTLD CHINC INKL MON+CH
FETCH0		0		FETCH0 MON INKL MON+CH
FETCH1		1		MON STFET1 INKL MON+CH
STORE0		0		FETCH0 MON INKL MON+CH
STORE1		1		MON STFET1 STORE1 INKL MON+CH

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BASIC INSTRUCTIONS	
SIGNAL	EQUATION
TC0	$\overline{SQEXT}$ SQ0 ST0
GOJ1	$\overline{SQEXT}$ SQ0 ST1
TCSAJ3	$\overline{SQEXT}$ SQ0 ST3
CCS0	$\overline{SQEXT}$ SQ1 QC0 ST0
TCF0	$\overline{SQEXT}$ SQ1 $\overline{QC0}$ ST0
OAS0	$\overline{SQEXT}$ SQ2 QC0 ST0
OAS1	$\overline{SQEXT}$ SQ2 QC0 ST1 + ADS0
LXCH0	$\overline{SQEXT}$ SQ2 QC1 ST0
INCR0	$\overline{SQEXT}$ SQ2 QC2 ST0
ADS0	$\overline{SQEXT}$ SQ2 QC3 ST0
NDX0	$\overline{SQEXT}$ SQ5 QC0 ST0
RSM3	$\overline{SQEXT}$ SQ5 QC0 ST3
DXCH0	$\overline{SQEXT}$ SQ5 QC1 ST0
TS0	$\overline{SQEXT}$ SQ5 QC2 ST0
AD0	$\overline{SQEXT}$ SQ6 ST0
MSK0	$\overline{SQEXT}$ SQ7 ST0

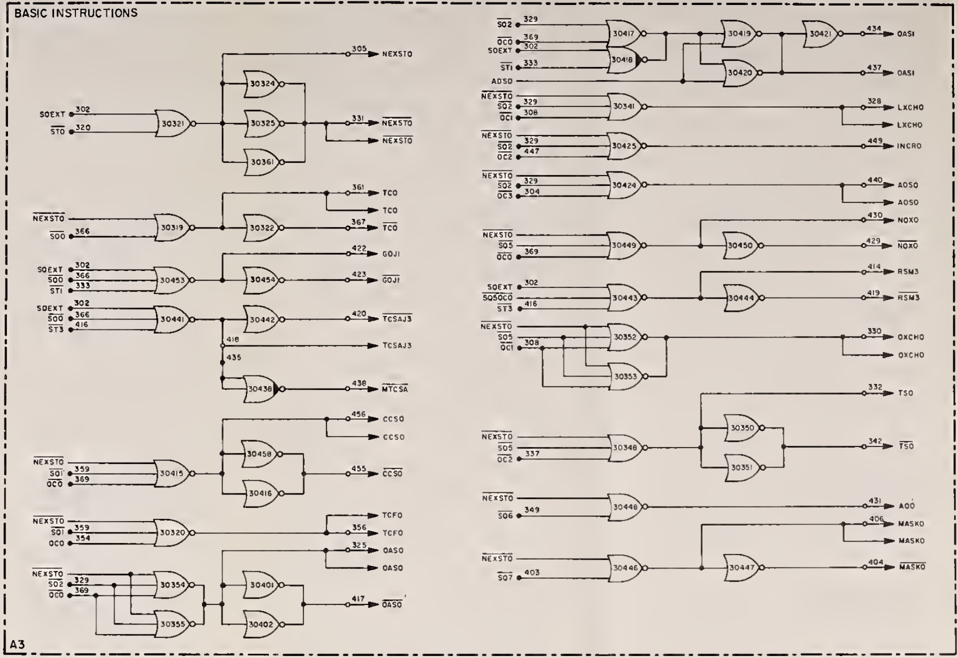

Figure 4-131. Subinstruction Decoder, Logic Diagram (Sheet 1 of 3)

CHANNEL INSTRUCTIONS	
SIGNAL	EQUATION
READ0	SQEXT SQ0 QC0 $\overline{\text{SQRI0}}$ ST0
WRITE0	SQEXT SQ0 QC0 SQRI0 ST0
RAND0	SQEXT SQ0 QC1 $\overline{\text{SQRI0}}$ ST0
WAND0	SQEXT SQ0 QC1 SQRI0 ST0
ROR0	SQEXT SQ0 QC2 $\overline{\text{SQRI0}}$ ST0
WOR0	SQEXT SQ0 QC2 SQRI0 ST0
RXOR0	SQEXT SQ0 QC3 $\overline{\text{SQRI0}}$ ST0
RUPT0	SQEXT SQ0 QC3 SQRI0 ST0
RUPT1	SQEXT SQ0 QC3 SQRI0 ST1

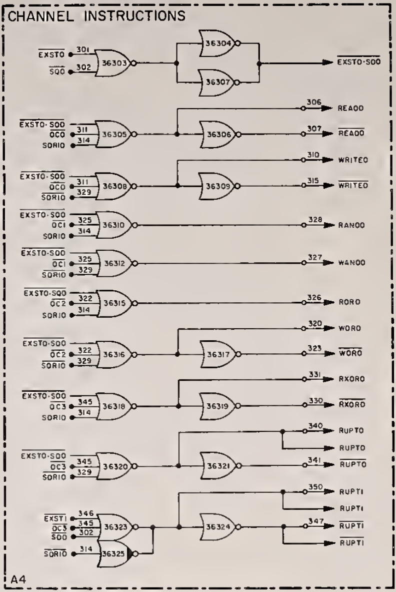

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Figure 4-131. Subinstruction Decoder, Logic Diagram (Sheet 2 of 3)

EXTRACODE INSTRUCTIONS	
SIGNAL	EQUATION
OV0	SQEXT SQ1 QC0 ST0
OV1	SQEXT SQ1 QC0 ST1
OV1376	SQEXT SQ1 QC0 ST1376
DV376	SQEXT SQ1 QC0 ST376
OV3764	SQEXT SQ1 QC0 ST3764
OV4	SQEXT SQ1 QC0 ST4
BZF0	SQEXT SQ1 $\overline{\text{QC0}}$ ST0
MSU0	SQEXT SQ2 QC0 ST0
QXCH0	SQEXT SQ2 QC1 ST0
AUG0	SQEXT SQ2 QC2 ST0
DIM0	SQEXT SQ2 QC3 · ST0
DCA0	SQEXT SQ3 ST0
DCS0	SQEXT SQ4 ST0
NOXX1	SQEXT SQ5 ST1
SU0	SQEXT SQ6 QC0 ST0
BZMF0	SQEXT SQ6 $\overline{\text{QC0}}$ ST0
MP0	SQEXT SQ7 ST0
MP1	SQEXT SQ7 ST1
MP3	SQEXT SQ7 ST3

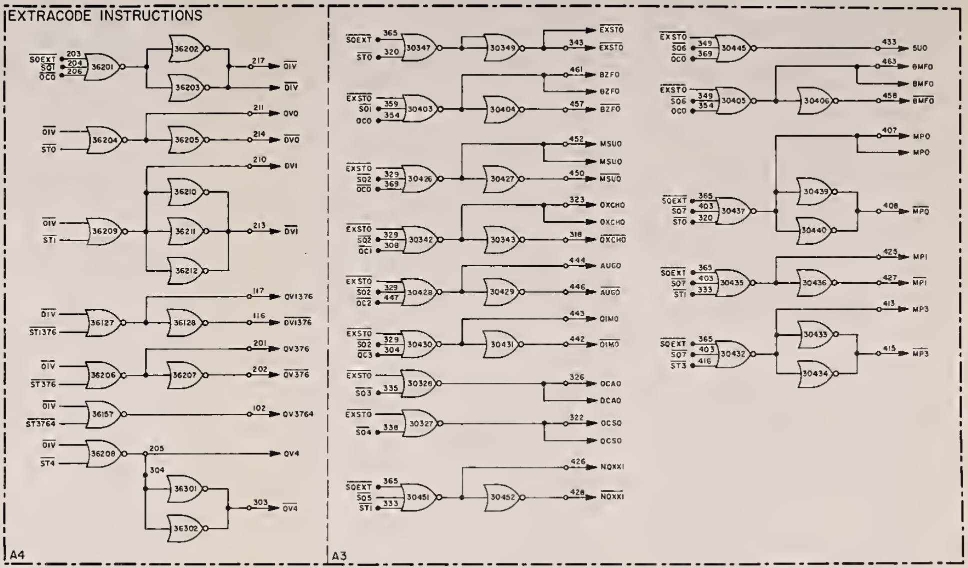

Figure 4-131. Subinstruction Decoder, Logic Diagram (Sheet 3 of 3)

without the QC signals. The basic instructions which can use any computer address are TC, CA, CS, AD, and MASK. The subinstruction commands produced without QC signals are TC0, AD0, and MASK0. Instructions CA and CS are controlled by instruction command signals from the instruction decoder.

The basic instructions which use the entire order code field are:

(1) CCS
(2) TCF
(3) DAD
(4) LXCH
(5) INCR
(6) ADS
(7) NDX
(8) RESUME
(9) DXCH
(10) TS
(11) XCH

These instructions have commands which are produced with a QC signal. Other important points concerning basic instructions are that signal DAS1 is an instruction command and signal LXCH0 is not used to produce crosspoint pulses.

Signal DAS1 is an instruction command because it is used for subinstructions DAS1 and ADS0. Subinstruction LXCH0 is controlled by instruction commands IC8 and IC9 which are produced by signal LXCH0. The logic diagram for basic instructions contains the circuits which produce commands TCSAJ3 and GOJ1. These commands are for peripheral and interrupt instructions, respectively, and are included here because they have order codes similar to basic instructions. Signal MTCSA is fed to the peripheral equipment.

The channel instructions and RUPT instruction are controlled by commands which are produced from the entire order code content of register SQ and the content of the stage counter. For example, when subinstruction WAND0 is to be executed, register SQ is set to the 1 000 011 state and the stage counter is set to 000. As a result, signals SQEXT, SQ0, QC1, and SQR10 are present and ANDed to produce subinstruction command WAND0.

The extracode instructions are also shown in figure 4-131. Special attention is given to the commands for the divide instruction because of the Gray code count used to control the commands. When instruction DV is to be executed, register SQ is set to the 1 001 00X state and the stage counter is set to 000. As a result, signals SQEXT, SQ1, QC0, and ST0 are supplied to the subinstruction decoder. Signals SQEXT, SQ1, and QC0 are ANDed to produce instruction command DIV. In addition, signals DIV and ST0 are ANDed to produce subinstruction command DV0. Since signal DIV is produced without an ST signal, it remains for the duration of the divide instruction. It is also used to produce subinstruction commands DV1 and DV4 and instruction commands DV1376, DV376, and DV3764. Subinstructions DV1, DV3, DV7, and DV6 start at time pulse T04 and end at the following time pulse T03. Instruction command DV1376 produces crosspoint pulse for time pulse T01, T02, and T03 whereas instruction command DV376 produces crosspoint pulses for time pulses T04 through T12. Instruction command DV3764 is not used to produce crosspoint pulses but it does turn off fixed memory timing during four MCT's of the divide instruction.

The remaining commands for the extracode instructions are similar to the commands for the basic instructions. Instructions DCA, DCS, NDXX, and MP do not encroach on the address field for their order codes. As a result, the commands for these instructions do not use a QC signal. Signals BZF0, DCS1, and BZMF0 are not used to produce crosspoint pulses but are used to produce instruction command signals which control the associated subinstructions.

4-5.4.8 Instruction Decoder. The instruction decoder receives the SQ and ST code signals from the order code processor and commands from the subinstruction decoder. The instruction decoder produces commands that are used for two or more subinstructions. These commands are ANDed with time pulses T01 through T12 as necessary to produce crosspoint pulses. Table 4-IX lists the commands produced for each subinstruction. Table 4-X lists the subinstructions that use a particular command for producing crosspoint pulses.

Table 4-X. Subinstructions Per Command

Command	Subinstructions	Command	Subinstructions
AD0	AD0	DIV	DV0 DV1 DV3 DV7 DV6
ADS0	ADS0	DV0	DV0
AUG0	AUG0	DV1	DV1
CCS0	CCS0	DV4	DV4
CHINC	INOTRD INOTLD	DV376	DV3 DV7 DV6
DAS0	DAS0	DV1376	DV1 DV3 DV7 DV6
DAS1	DAS1 ADS0	DXCH0	DXCH0
DCA0	DCA0		
DCS0	DCS0		
DIM0	DIM0		
DINC	DINC		

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Table 4-X. Subinstructions Per Command

Command	Subinstructions
FETCH0	FETCH0 STORE0
GOJ1	GOJ1
IC1	NDX0 NDXX0
IC2	NDX1 NDXX1
IC3	STD2 TC0 TCF0
IC4	DCA0 DCS0
IC5	DXCH1 XCH0
IC6	CA0 DCA1
IC7	CS0 DCS1
IC8	LXCH0 DXCH0
IC9	LXCH0 DXCH1 TS0 XCH0 QXCH0 DAS0
IC10	DXCH0 DCA0 DCS0
IC11	AD0 SU0 CCS0
IC12	MSU0
IC13	CA0 CS0 NDX0 AD0 DCA0 DCA1 DCS0 DCS1 NDXX0 SU0
IC14	MASK0 MP0 RXOR0
IC15	BZF0 BZMF0
IC16	BZF0 BZMF0
IC17	BZF0 BZMF0
INCR0	INCR0
INKL	PINC MINC PCDU MCDU DINC SHINC SHANC INOTRD INOTLD FETCH0 FETCH1 STORE0 STORE1

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Table 4-X. Subinstructions Per Command

Command	Subinstructions	Command	Subinstructions
INOTLD	INOTLD	PARTC	PINC MINC PCDU MCDU DINC
INOUT	READ0 WRITE0 RAND0 WAND0 ROR0 WOR0 RXOR0	PCDU	PCDU
MASK0	MASK0	PINC	PINC
MCDU	MCDU	PRINC	INCR0 AUG0 DIM0
MINC	MINC	QXCH0	QXCH0
MON	FETCH0 FETCH1 STORE0 STORE1	RAND0	RAND0
MON+CH	INOTRD INOTLD FETCH0 FETCH1 STORE0 STORE1	READ0	READ0
MP0	MP0	ROR0	ROR0
MP1	MP1	RSM3	RSM3
MP3	MP3	RUPT0	RUPT0
MSU0	MSU0	RUPT1	RUPT1
NDX0	NDX0	RXOR0	RXOR0
NDXX1	NDXX1	SHANC	SHANC
		SHIFT	SHINC SHANC
		STD2	STD2
		STFET1	FETCH1 STORE1

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Table 4-X. Subinstructions Per Command

Command	Subinstructions	Command	Subinstructions
STORE1	STORE1	TCSAJ3	TCSAJ3
SU0	SU0	TS0	TS0
		WAND0	WAND0
TC0	TC0	WOR0	WOR0
TCF0	TCF0	WRITE0	WRITE0

(Sheet 4 of 4)

Figure 4-132 shows the logic circuits that produce most of the instruction commands for basic, channel, extracode, counter, and peripheral instructions. Two examples are used to describe how the instruction commands are produced. First, consider signal IC5 which is used for subinstructions DXCH1 and XCH0. When subinstruction DXCH1 is to be executed the order code content of register SQ is 0 101 01X and the stage counter is set to 001. As a result, signals SQ5, QC1, and ST1 are present. Since the high order bit is a logic ZERO, signal SQEXT is not present. These conditions are detected by an AND function and signal IC5 is produced. When subinstruction XCH0 is to be executed signals SQ5, QC3, and ST0 are present and signal SQEXT is not present. These conditions are also detected by an AND function and signal IC5 is produced.

The second way to produce instruction command signals is by ORing various subinstruction commands. For example, signal IC12 is produced by subinstruction command CCS0 or MSU0. Another example is signal IC10 which is produced by subinstruction command DXCH0 or DAS0. It is also produced by instruction command signal IC4. Commands IC16 and IC17 are dependent on branch conditions. Signal IC16 is produced by signals BZF0 and BR2 or by signals BZMF0 and either BR1 or BR2. Signal IC17 is produced when signal IC16 is not present because of improper branch conditions during subinstructions BZF0 and BZMF0.

INSTRUCTION DECODER	
SIGNAL	EQUATION
IC1	SQEXT SQ5 ST0 + SQ5 QC0 · ST0
IC2	SQEXT SQ5 ST1 + SQ5 QC0 ST1
IC3	TC0 + TCF0 + ST02
IC4	DCA0 + DCS0
IC5	$\overline{SQEXT}$ SQ5 QC1 ST1 + $\overline{SQEXT}$ SQ5 QC3 ST0
IC6	$\overline{SQEXT}$ SQ3 ST0 + SQEXT SQ3 ST1
IC7	$\overline{SQEXT}$ SQ8 ST0 + SQEXT SQ8 ST1
IC8	OXCH0 + LXCH0
IC9	IC5 + TS0 + LXCH0 + QXCH0
IC10	IC4 + OXCH0 + DAS0
IC11	$\overline{SQEXT}$ SQ6 ST0 + SQ6 QC0 ST0
IC12	CCS0 + MSU0
IC13	IC1 + IC5 + IC7 + IC11 + DCS0 + DCA0
IC14	MP0 + RXOR0 + MASK0
IC15	BZF0 + BMF0
IC16	BZF0 · BR2 + BMF0 (BR1 + BR2)
IC17	IC15 · $\overline{IC16}$
INOUT	SQEXT SQ0 ST0 · $\overline{RUPT0}$
PRINC	SQ2 $\overline{QC3}$ ST0 + SQEXT · SQ2 SQR12 ST0
PARTC	INKL SHIFT (MON + CH)

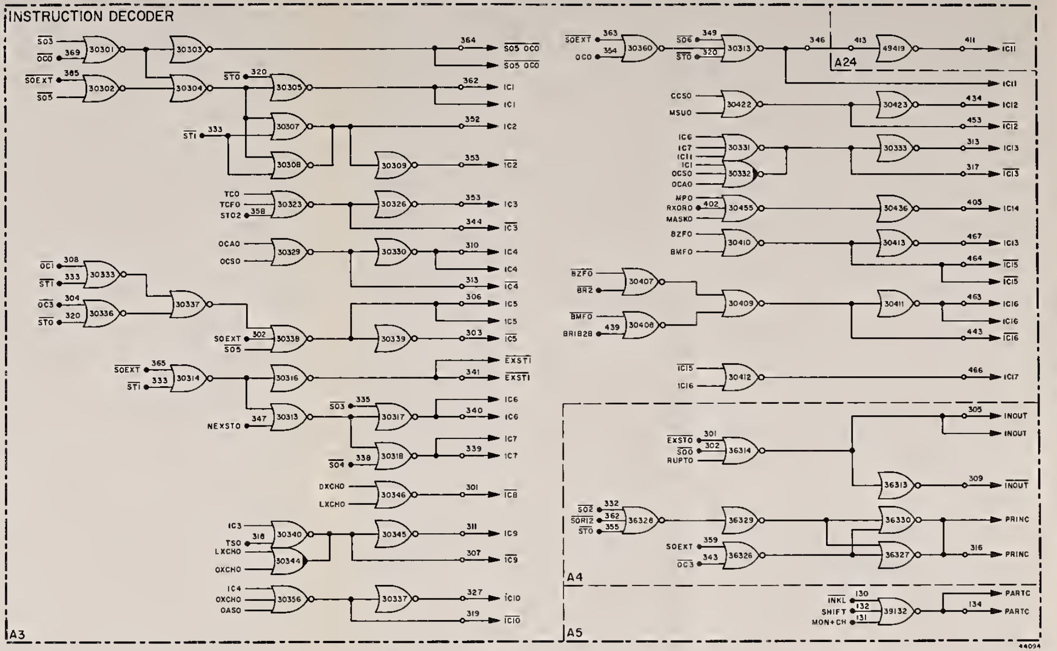

Figure 4-132. Instruction Decoder, Logic Diagram

4-5.4.9 Counter and Peripheral Instruction Control. The counter and peripheral instruction control (figure 4-133) is regulated by signals from the priority control and peripheral equipment. The signals supplied by the priority control are the start order code signal (GOJAM), the counter OR signal (CTROR), and the various counter increment signals that request a particular counter instruction. The prime function of signal GOJAM is to take top priority by inhibiting and resetting many circuits in the counter and peripheral instruction control. Signal CTROR is used to produce the increment signal (INKL) in addition to various strobe signals. The signals supplied by the peripheral equipment are MREAD, MLOAD, MRDCH, MLDCH for FETCH, STORE, INOTRD, and INOTLD instructions, respectively. The peripheral equipment also supplies signal MNHNC for inhibiting the counter increment operation. The counter and peripheral instruction control supplies the following subinstruction commands to the control pulse generator:

(1) STORE1
(2) PINC
(3) MINC
(4) PCDU
(5) MCDU
(6) SHINC
(7) SHANC
(8) DINC

It also supplies the following instruction commands:

(1) INKL
(2) STFET1
(3) MONTCH
(4) CHINC
(5) FETCH0

The instruction command signal INKL must always be produced before a counter or peripheral instruction can be executed. Signal INKL interrupts the operation of the register SQ control, SQ decoder, and stage decoder so that no instruction or subinstruction command will be produced while the counter or peripheral instruction is being executed. Signal INKL does not destroy the order code in register SQ; it simply delays recognition of the order code until the counter or peripheral instruction has been executed.

A counter or peripheral instruction cannot be executed if a GOJAM condition exists. Signal GOJAM is applied to the set side of the GNHNC flip-flop. If time pulse T01 is not present, signal GOJAM will set the GNHNC flip-flop. The flip-flop will remain set until the following T01 time pulse. Signal B controls the time at which a counter or peripheral instruction can be executed. Signal B is present at time pulse T12 provided signal NISQL is also present. Signal NISQL is produced by the register SQ control. This signal is present only at the end of each instruction; its absence at time pulse T12 prevents a counter or peripheral instruction from being executed between subinstructions. Signal B is produced during the last quarter interval of time pulse T12 as indicated by the presence of signal PHS4.

When a counter instruction is to be executed, signal CTROR from the priority control is present. The presence of signals B and CTROR will allow a counter increment to occur provided the operation is not manually inhibited by signal MNHNC from the peripheral equipment or by signal A. Signal A is produced whenever a peripheral instruction is to be executed and gives the peripheral instructions priority over the counter instructions. If the preceding conditions are met, flip-flop C will set. The set input to flip-flop C can be overridden by signal GOJAM if both the set and reset inputs occur at the same time. Signal C will be present for almost a full MCT, starting during the last quarter interval of time pulse T12 and remaining until the third quarter interval of the following T12 pulse. The third quarter reset interval is controlled by signal PHS3. If additional counter incrementing is to take place, the C flip-flop will remain set. It can be reset any time by signal GOJAM or at time pulse T12 if both a counter and a peripheral instruction are requested at the same time. When this happens, signal A in addition to signals T12 and PHS3 will reset the C flip-flop. At the end of all counter incrementing, the absence of signal CTROR will cause the flip-flop to reset at time pulse T12.

Signal INKL is produced directly from signal C or from signal MON+CH which indicates a peripheral instruction is being executed. Signal C also produces signal INCSET at time pulse T02 and signal RSSB during the third quarter of time pulse T07. Signal INCSET causes any counter instruction request to set the associated counter instruction flip-flop. Signal RSSB in conjunction with decoded counter addresses, resets cells in the priority control. This action terminates counter instruction requests applied to the counter and peripheral instruction control. Signal MINKL is sent to the peripheral equipment and can be used to produce a time pulse T12 stop and turn on an indicator.

Signal A is present when a peripheral instruction is to be executed. The A flip-flop may be set by signal MREAD, MLOAD, MRDCH, or MLDCH from the peripheral equipment. These signals are subjected to the timing of signal PHS2. The flip-flop remains set until the T11 time pulse, during which signal MON+CH is present. The A flip-flop is also reset by signal GOJAM, which may occur at any time.

Signal A resets the C flip-flop at the next T12 time pulse. It is also used to establish a peripheral instruction request. A peripheral instruction cannot be executed before the completion of the current instruction. This action is controlled by signal B which is produced at time pulse T12 when the NISQL flip-flop is set. Signal A is produced by signal MLDCH when the channel load instruction INOTLD is to be executed. Signals MLDCH, A, and B cause the INOTLD flip-flop to set. The channel load instruction is one MCT long. Therefore, the INOTLD flip-flop remains set for one MCT from the last quarter of time pulse T12 as determined by signal B to the second quarter of the following T12 time pulse as determined by reset signals T12 and PHS2. The channel read instruction is controlled by flip-flop INOTRD which is set by signals MRDCH, A, and B and reset by signals T12 and PHS2. The timing of signals INOTLD and INOTRD is identical. These signals are subinstruction commands and either one will produce instruction commands signals CHINC and MON+CH. Signal MON+CH, in turn, produces signal INKL and also causes the A flip-flop to be reset at time pulse T11.

Instructions STORE and FETCH are both two MCT's long. The STORE flip-flop is set when signals MLOAD, A, and B are all present and signal GOJAM is not present. The STORE flip-flop remains set for two MCT's. During the first MCT, the stage counter is set to the 000 state and produces signal ST0. Signal STORE produces signal MON which in turn is combined with signal ST0 to produce instruction command signal FETCH0. During the second MCT, the stage counter is set to the 001 state and produces signal ST1. Signals STORE and ST1 are then combined to produce subinstruction command

PERIPHERAL INSTRUCTION	
SIGNAL	EQUATION
A	(MREAD + MLOAD + MRDCH + MLOCH) PHS2 $\overline{GOJAM}$ + A $\overline{GOJAM}$ $\overline{T11}$ $\overline{(MON + CH)}$
GNHNC	(GOJAM + GNHNC) $\overline{T01}$
B	GNHNC · T12 · NISQL · PHS4 · $\overline{PSEUDO}$
C	$\overline{B\ CTROR\ \overline{A}\ \overline{MNHNC}}$ $\overline{GOJAM}$ + C $\overline{GOJAM}$ $\overline{T12\ PHS3\ CTROR\ \overline{A}}$
INCSET	T02 C
RSSB	T07 C PHS3
INKL	C + MON + CH
INOTLD	MLOCH A B + INOTLD $\overline{T12\ PHS2}$
INOTRD	MRDCH A B + INOTRD $\overline{T12\ PHS2}$
CHINC	$\overline{INOTLD}$ $\overline{INOTRD}$
STORE	MLOAD A B $\overline{GOJAM}$ + STORE $\overline{GOJAM}$ $\overline{T12\ PHS2\ MON\ ST1}$
STORE1	STORE ST1
FETCH	MREAD A B $\overline{GOJAM}$ + FETCH $\overline{GOJAM}$ $\overline{T12\ PHS2\ MON\ ST1}$
FETCH1	FETCH ST1
STFET1	STORE1 + FETCH1
MON	$\overline{STORE}$ $\overline{FETCH}$
FETCH0	MON ST0
MON + CH	STORE + FETCH + INOTLD + INOTRD

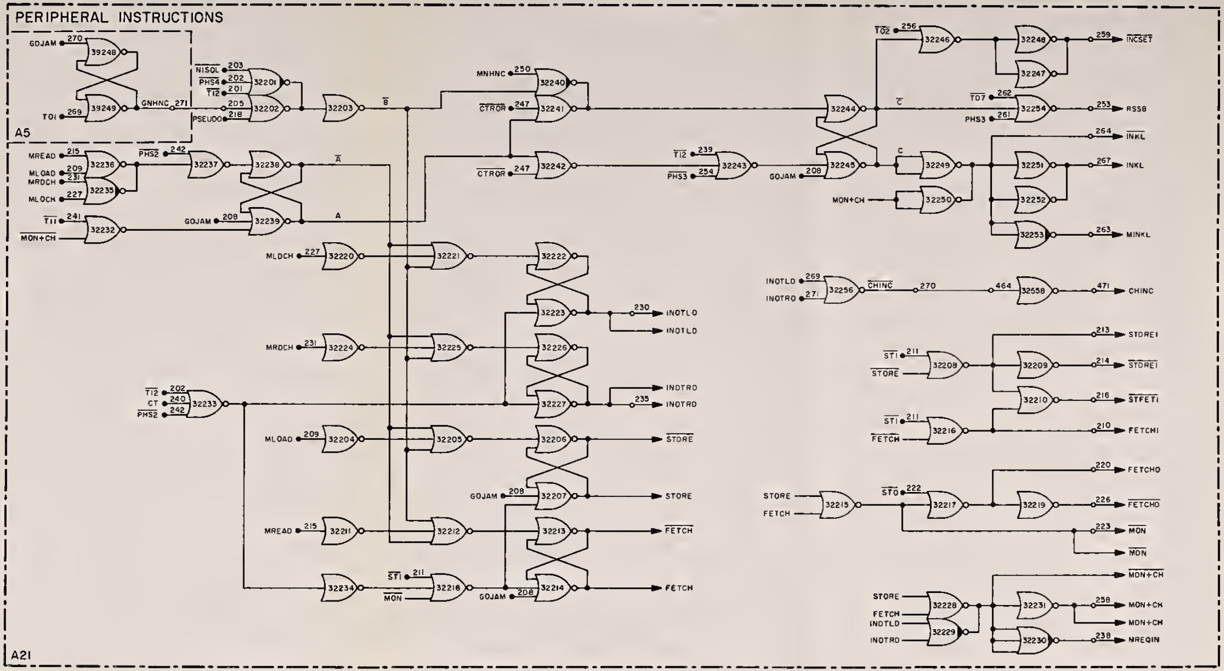

Figure 4-133. Counter and Peripheral Instruction Control Logic (Sheet 1 of 2)

COUNTER INSTRUCTIONS	
SIGNAL	EQUATION
PINC	(C24A + C25A + C26A + C27A + C30A + C37P + C40P + C41P + C42P + C43P + C44P) INCSET + PINC $\overline{\text{T12}}$
MINC	(C37M + C40M + C41M + C42M + C43M + C44M) INCSET + MINC $\overline{\text{T12A}}$
PCDU	(C32P + C33P + C34P + C35P + C36P) INCSET + PCDU $\overline{\text{T12A}}$
MCDU	C32M + C33M + C34M + C35M + C36M) INCSET + MCDU $\overline{\text{T12A}}$
SHINC	(C45M + C46M + C57A + C60A) INCSET + SHINC $\overline{\text{T12A}}$
SHANC	(C45P + C46P) INCSET + SHANC $\overline{\text{T12A}}$
DINC	(C31A + C47A + C50A + C51A + C52A + C53A + C54A + C55A + C56) INCSET + DINC $\overline{\text{T12A}}$

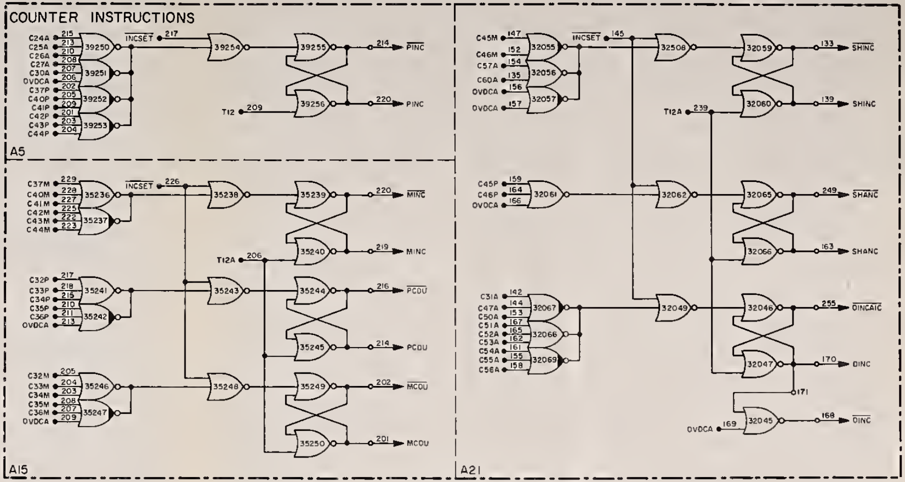

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Figure 4-133. Counter and Peripheral Instruction Control Logic (Sheet 2 of 2)

signal STORE1. In addition, when signals T12, PHS2, MON, and ST1 are all present, the STORE flip-flop is reset. This condition occurs at the end of the second MCT. Signal STORE also produces signal MON+CH which resets the A flip-flop at time pulse T11. The STORE flip-flop may be reset at any time by signal GOJAM.

The FETCH flip-flop is set when signals MREAD, A, and B are present. Signal FETCH produces signals MON and MON+CH. During the first MCT of instruction FETCH, signal MON and ST0 produce instruction command FETCH0. During the second MCT, signals FETCH and ST1 produce signal FETCH1. Instruction command STFET1 is produced by either FETCH1 or STORE1. The FETCH flip-flop is reset at time pulse T12 when signals PHS2, MON, and ST1 are all present. It may also be reset by signal GOJAM. Signal MREQIN is sent to the peripheral equipment to indicate that the computer has accepted the instruction request and to control the circuits which supply signals MREAD, MLOAD, MRDCH, and MLDCH.

The priority control supplies instruction signals to the counter and peripheral instruction control. The priority control contains 29 counter cell circuits, one for each counter location in erasable memory. Each counter performs a particular function. For example, time counters T1 through T5 are incremented at regular intervals to provide elapsed time data for the program. Since these counters can only be incremented, they are controlled by instruction PINC. Other counters can be incremented or decremented by instructions PINC or MINC, respectively, or by instructions PCDU or MCDU when dealing with the CDU counters. Other counters are controlled by instructions SHINC, SHANC, and DINC.

When any counter is to be updated the associated cell in the priority control is set by an incremental pulse input. The cell then produces a counter address signal. For example, if the counter at location 0024 is to be updated, cell 24 is set and counter address signal C24A is produced. The counter address signal then performs as many as two functions. First, if the counter being updated is controlled by only one instruction such as instruction PINC, the counter address signal sets the associated instruction flip-flop in the counter and peripheral instruction control. Then, as the instruction is being executed, the counter address signal produces the corresponding octal address which is placed onto the write lines and written into register S by control pulse action.

Since certain counters are controlled by two instructions, their counter address signals cannot be used to set an instruction flip-flop in the counter and peripheral instruction control. The cells in the priority control for these counters produce one of two signals in addition to the counter address signal. The additional signals are produced by flip-flop in the cell circuit. If a counter is to be decremented, one of the two flip-flops will be set by an incremental input. If the same counter must be incremented at later time, the other flip-flop is set by a different incremental input. The signals from these flip-flops are labeled with a P or an M to indicate a plus increment or minus increment, respectively. For example, when counter 0037 is being incremented, signal C37P is produced. This signal sets the PINC flip-flop in the counter and peripheral instruction control. When the same counter is being decremented, signal C37M is produced. This signal sets the MINC flip-flop. Table 4-IX lists the counter address and instruction signals from the cells in the priority control.

Table 4-XI. Counter Cell Signals

Counter	Location	Address Signal	Instruction Signal	Instruction
T2	0024	C24A		PINC
T1	0025	C25A		PINC
T3	0026	C26A		PINC
T4	0027	C27A		PINC
T5	0030	C30A		PINC
T6	0031	C31A		DINC
CDUX	0032	C32A	C32P	PCDU
			C32M	MCDU
CDUY	0033	C33A	C33P	PCDU
			C33M	MCDU
CDUZ	0034	C34A	C34P	PCDU
			C34M	MCDU
TRN	0035	C35A	C35P	PCDU
			C35M	MCDU
SHAFT	0036	C36A	C36P	PCDU
			C36M	MCDU
PIPX	0037	C37A	C37P	PINC
			C37M	MINC
PIPY	0040	C40A	C40P	PINC
			C40M	MINC
PIPZ	0041	C41A	C40P	PINC
			C40M	MINC
BMAGX	0042	C42A	C42P	PINC
			C42M	MINC
BMACY	0043	C43A	C43P	PINC
			C43M	MINC
BMACZ	0044	C44A	C44P	PINC
			C44M	MINC
INLINK	0045	C45A	C45P	SHANC
			C45M	SHINC
RNRAD	0046	C46A	C46P	SHANC
			C46M	SHINC
CYRO	0047	C47A		DINC
CDUX	0050	C50A		DINC
CDUY	0051	C51A		DINC
CDUZ	0052	C52A		DINC
TRUN	0053	C53A		DINC
SHAFT	0054	C54A		DINC
THRST	0055	C55A		DINC
EMS	0056	C56A		DINC
OTLINK	0057	C57A		SHINC
ALT	0060	C60A		SHINC

The cell signals which set the various counter flip-flops are shown in figure 4-133. Only one cell signal is present at a time. Each of the counter instruction flip-flops are set at time pulse T02 as determined by signal INCSET. Signal INCSET is present only when the NISQL flip-flop is set and no peripheral instruction is being executed. The counter instruction flip-flops remain set from time pulse T02 through T12. The control pulses required at time pulse T01 of the counter instructions are produced by instruction command signal INKL.

4-5.4.10 Crosspoint Generator. The crosspoint generator receives subinstruction and instruction commands from the command generator, branch commands from the branch control, and timing pulses from the timer. It produces crosspoint or action pulses as necessary by ANDing a given command signal with the appropriate time pulse signal. The crosspoint pulses are converted into control pulses and applied to various elements of the computer for regulating data flow. Some of the crosspoint pulses are used directly as control pulses due to the function which they must perform. However, most control pulses are produced by the control pulse gates. Some crosspoint pulses are controlled by branch commands in addition to a subinstruction or instruction command. For example, subinstruction CCS0 uses branch commands during time pulses T07 and T10 as listed in table 4-VII, Machine Instructions, paragraph 4-5.2.

Subinstruction CCS0 is a decision-making subinstruction. At time pulse T01, instruction command IC12 and time pulse T01 are ANDed to produce crosspoint pulse (XP) RL10BB as shown in figure 4-134 and listed in table 4-XII. Crosspoint pulse RL10BB is also produced by commands DAS0, DAS1, IC9, DXCH0, PIRNC, or INOUT. This pulse performs several functions. First, it is used as a control pulse to place the ten (10) low order bits of register B onto the write lines. Second, it is converted into control pulse (CP) WS which enters the content of the write lines into register S.

At time pulse T02, crosspoint pulse 2B is produced and converted into control pulses RSC and WG. Signal 2B is produced involuntarily every T02 time pulse except when inhibited by subinstruction commands MP1, MP3, or DV0 or instruction commands INOUT, IC15, and DV1376. Many subinstructions use control pulses RSC and WG at time pulse T02 as listed in table 4-VII. If the content of register S is an erasable memory address, control pulse WG clears register G and the decoded address signals inhibit control pulse RSC. Data from fixed or erasable memory may be transferred into it at a later time. If a central processor register is addressed, fixed and erasable memory timing is turned off, and the content of addressed register is copied into register G by control pulses RSC and WG. For subinstruction CCS0, the address in register S can be that of an erasable memory or central processor location. It can never be a fixed memory address because control pulse RL10BB does not place bits 12 and 11 of the address onto the write lines.

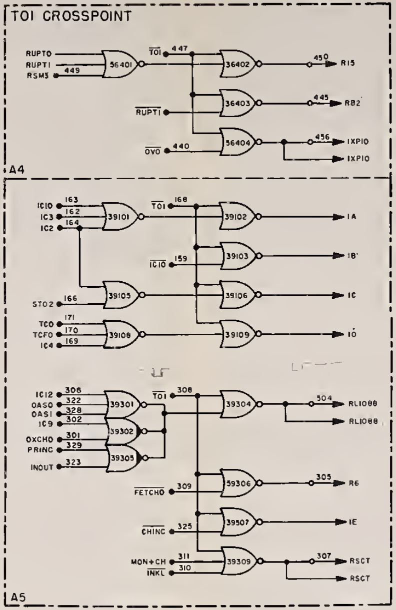
No crosspoint or control pulses are produced at time pulses T03 and T04 of subinstruction CCS0. However, the content of the addressed erasable memory location is entered into register G at time pulse T04.

Table 4-XII. Subinstruction CCS0

Time	BR1 and BR2	Involuntary		CCS0		IC12	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5				5G	RG TMZ TPZG TSGN	5J	RG WB
7	XX			7D	RZ WY12		
7	X1			7XP4	PONEX		
7	1X			PTWOX			
8		8XP10	WS	8A	RU WZ		
9						9B	RB WG
10	XX			10B	ST2 WY		
10	00			10XP9	RB		
10	X0			10XP6	CI MONEX		
10	1X			10G	RC		
11				11E	RU WA		

T01 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
R15	N15 WS	T01 (RSM3 + RUPT0 + RUPT1)
RB2	RB2	T01 RUPT1
1XP10	RA TMZ TSGN WB	T01 DVD
1A	CI WY12	T01 (IC2 + IC3 + IC10)
1B	MONEX	T01 IC10
1C	RZ	T01 (IC2 + STD2)
1D	RB	T01 (TC0 + TCF0 + IC4)
RL10BB	RL10BB WS	T01 (IC12 + OAS0 + OAS1 + IC9 + DXCH0 + PRINC + INDUT)
R6	R6 WS	T01 FETCH0
1E	RS	T01 CHINC
RSCT	RSCT WS	T01 INKL $\overline{\text{MON + CH}}$

T02 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
2A	WG	T02 WRITE0
2XP3	RA WB	T02 INOUT
2B	RSC WG	T02 $\overline{\text{(INOUT + MP1 + MP3A + DV0 + IC15 + OV1376)}}$
2XP5	RC TMZ WA	T02 DV0 · $\overline{\text{BR1}}$
2C	N1SQ	T02 (IC2 + IC3 + RSM3)
OVST	OVST	T02 OIV $\overline{\text{STO2}}$
2XP7	N1SQ ZIP	T02 MP3
2XP8	STL WY	T02 FETCH0



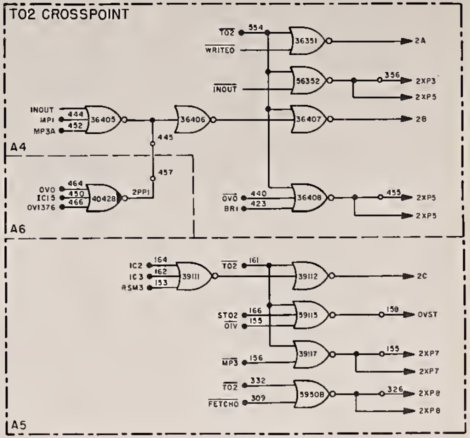


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Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 1 of 10)

T03 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
RRPA	RRPA WZ	T03 RUPTI
3XP7	RC RCH	T03 RXORO
3A	RB	T03 (RORO + WORO)
3B	RC	T03 (RANDO + WANDO)
3C	TSGN	T03 MPO
3D	WY	T03 INOUT
3XP2	TOV	T03 TSO
3XP5	RB WZ	T03 IC2
3E	RA TMZ TSGN WG	T01 IC15
3XP6	RZ WQ	T03 TCO
3F	RA WB	T03 (OASO + TSO + MASKO + IC5 + MPO)
3G	RL WB	T03 IC8
RQ	RQ WB	T03 QXCHO

T04 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
4A	CI L16	T04 TSO (BR1 BR2 + $\overline{BR1}$ $\overline{BR2}$)
4B	RB WL	T04 MPO · $\overline{BR1}$
4C	RC WL	T04 MPO BR1
4XP5	RZ WY12	T04 · TSO
4D	TSGN	T04 OV1 BR2
4XP11	RCH	T04 INOUT
4E	RSC WC	T04 UP3
4F	RA	T04 IC2
4G	TPZG	T02 IC15
4H	RL WA	T04 OASO
4J	RC WA	T04 MASKO
4K	RL	T04 OV1
4L	WB	T04 (OV1 + INOUT + IC2)
4M	WSC	T04 MON $\overline{FETCHI}$

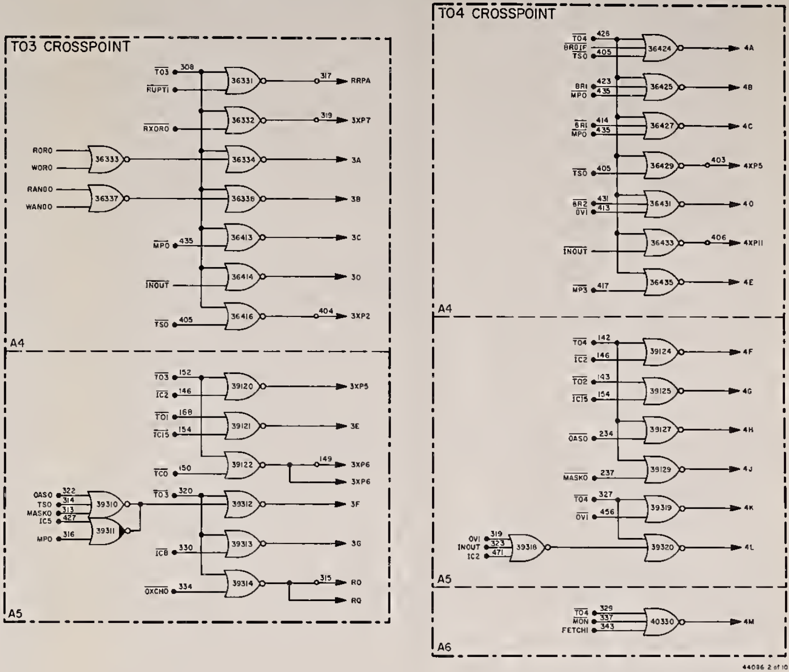

Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 2 of 10)

TO5 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
5XP28	RG TSGU WB	T05 DV4
5XP11	RU WA	T05 INOUT $\overline{READO}$ $\overline{WRITEO}$ $\overline{RXORO}$
5A	RB	T05 READO
5B	RA WCH	T05 WRITEO
5C	WCH	T05 WORO
5D	RA RC WG	T05 RXORO
5E	RB1	T05 TS0 BR1 $\overline{BR2}$
5F	R1C	T05 TS0 BR1 $\overline{BR2}$
B15X	CI5X WY	T05 DV1
5XP4	RG WZ	T05 RSM3
5G	RG TMZ TPZG TSGN	T05 (PARTC + PRINC + CCS0)
5H	RZ	T05 IC2
5XP12	RU WL	T05 DAS0
TRSM	TRSM	T05 NDX0

TO5 CROSSPOINT (cont)		
SIGNAL	CONTROL PULSES	EQUATION
5J	RG WB	T05 IC12
5K	RG A2X	T05 DAS1
5L	WY	T05 (PRINC + DAS1 + PARTC)
5XP9	RG TSGN WYD	T05 SHIFT
5M	CI	T05 SHANC
5XP13	RG WL	T05 IC8
5XP15	RG WQ	T05 QXCH0
5XP21	RCH	T05 CHINC
5N	CI RB WY12	T05 IC16
5P	CI RZ WY12	T05 MP3
5Q	RG	T05 IC5
5R	RC	T05 (DV1 BR1 + RAND0 + WAND0)
Z16	Z16	T05 DV1 BR1
5XP19	RB	T05 (DV1 $\overline{BR1}$ + ROR0 + WOR0)
5S	WA	T05 TS0 ($\overline{BR1}$ BR2 + BR1 $\overline{BR2}$) + T05 (IC2 + IC5 + READO + DV4)

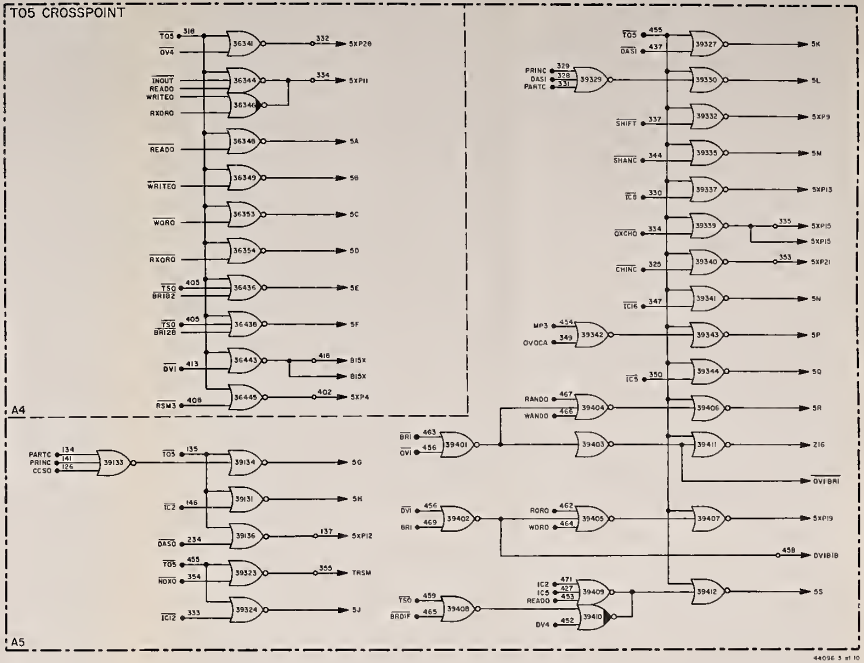

Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 3 of 10)

T06 CROSSPOINT

SIGNAL	CONTROL PULSES	EQUATION
6XP5	RU TOV WL	T06 OV1
TL15	TL15	T06 MP3
6A	RB WG	T06 RSM3
6B	A2X RG WY	T06 DAS0
6C	A2X CI RC WY	T06 MSU0
6D	RU WZ	T06 (IC16 + MP3 + IC2 + IC3 + TS0)
6XP8	RU TOV WG WSC	T06 DAS1
6XP7	RZ TOV	T06 OV4
6XP2	RA WB	T06 $\overline{RXOR0}$ INOUT
6XP10	PONEX	T06 (AUG0 $\overline{BR1}$ + DIM0 BR1 $\overline{BR2}$ + DINC BR1 $\overline{BR2}$ + INCR0 + PINC)
6E	MONEX	T06 (MINC + MCDU + AUG0 BR1 + DIM0 $\overline{BR1}$ $\overline{BR2}$ + DINC $\overline{BR1}$ $\overline{BR2}$)
6XP12	CI	T06 (PCDU + MCDU)

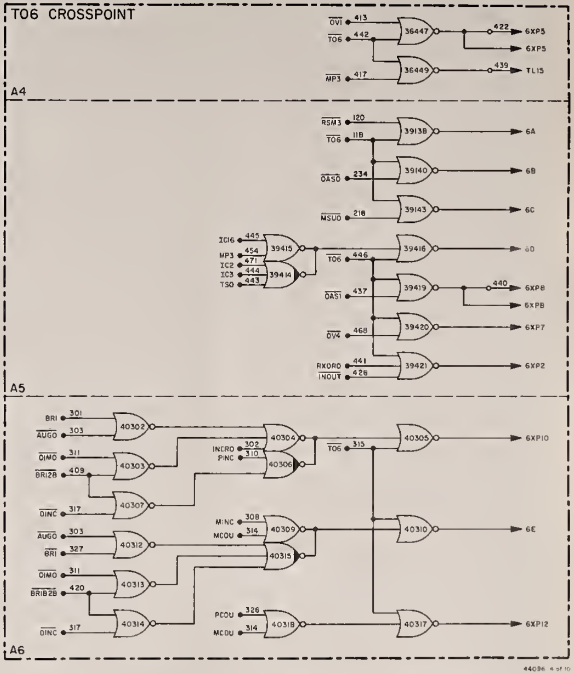

Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 4 of 10)

T07 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
TSGN2	TSGN2	T07 MP0
7A	RSC TSGN	T07 OV1
7XP19	A2X RB WY	T07 MP3 BR1
7B	RB	T07 DASO
7XP9	RUS TSGN	T07 MSU0
7C	A2X NG WY	T07 IC2
7XP4	PONEX	T07 CCS0 BR2
PTWOX	PTWOX	T07 CCS0 BR1
7D	RZ WY12	T07 CCS0
7E	NG	T07 STFET1
7F	NG WB	T07 (IC13 + IC14 + OV1)
7G	WA	T07 (OAS0 + OAS1 + MSU0)
7XP7	RC WA	T07 OV4 (BR1 + BR2) + T07 (RAND0 + WAND0)
7XP14	WCH	T07 (INOTLD + WAND0)
7XP10	RB1	T07 OAS1 (BR1 + $\overline{BR2}$)
7XP11	R1C	T07 OAS1 ($\overline{BR1}$ + BR2)
7XP15	RUS	T07 (PCDU + MCDU + SHIFT)
7H	RU	T07 (PRINC + PINC + MINC + DINC)
WOVR	WG WOVR WSC	T07 (MON + CH) (PRINC + INKL)
7J	RB WC WSC	T07 (IC9 + OXCH0)

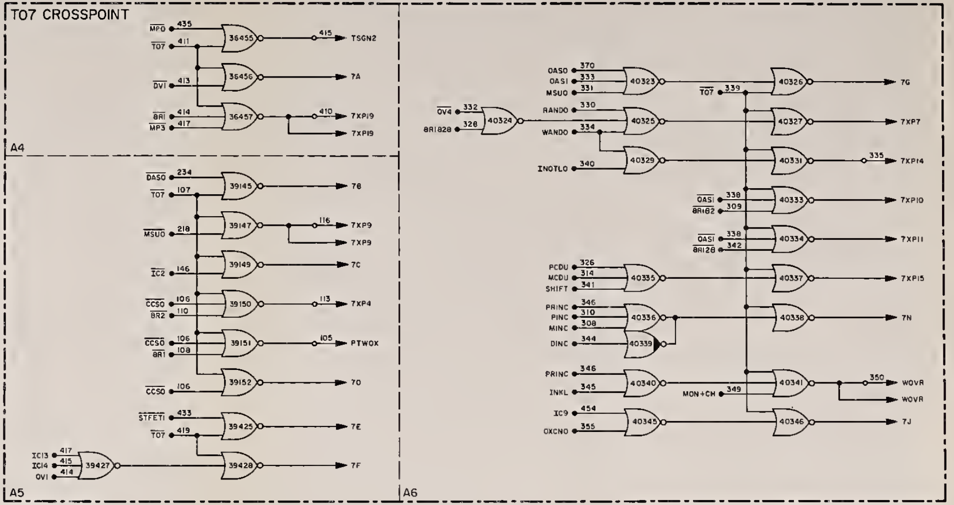

Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 5 of 10)

T08 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
8A	RU WZ	T08 CCS0
8B	RB	T08 INKL $\overline{\text{FETCH0}}$
RAD	RAD WB	T08 (IC3 + RSM3 + MP3 + IC16)
8XP15	NISQ	T08 IC16
8XP3	RZ	T08 (MP0 + IC1)
8C	RU	T08 (IC2 + IC4 + DXCH0)
8D	WB	T08 (GOJ1 + DAS0 + DXCH0)
RSTRT	RSTRT	T08 GOJ1
8XP12	RL	T08 DAS0
8E	ST2 WZ	T08 TCSAJ3
U2BBK	U2BBK	T08 $\overline{\text{MONWBK}}$ STFET1
RSTSTG	RSTSTG TSGN	T08 DV4
8XP4	RZ ST2	T08 (RUPT1 + DAS1 + MSU0 + IC17 + MASK0 + IC11 + IC6 + IC7 + IC9 + INOUT + DV4 + PRINC)
8XP10	WS	T08 $\overline{\text{RUPT0}}$ $\overline{\text{DAS0}}$ $\overline{\text{MP1}}$ $\overline{\text{DV1376}}$
8XP5	RA WY	T08 DV1
8XP6	PONEX	T08 DV1 $\overline{\text{BR2}}$

T09 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
9XP1	RG WG	T09 RUPT0
9A	RC WG	T09 RXOR0
9B	RB WG	T09 (RUPT1 + IC13 + IC12)
9C	WG	T09 STORE1
9D	RB WY	T09 MP0 $\overline{\text{BR1}}$
9E	RC WY	T09 MP0 BR1
9F	CI	T09 MP0 ($\overline{\text{BR1}}$ BR2 + BR1 $\overline{\text{BR2}}$)
9G	RA	T09 MP3
KRPT	KRPT	T09 RUPT1
9H	RB WA	T09 (IC2 + DV1 $\overline{\text{BR1}}$)
9XP5	RU TOV WG WSC	T09 DAS0
9J	RA RC WY	T09 MASK0
9K	RC WA Z15	T09 DV4
9L	RU WB WL	T09 DV4
9M	RC TMZ	T09 DAS1

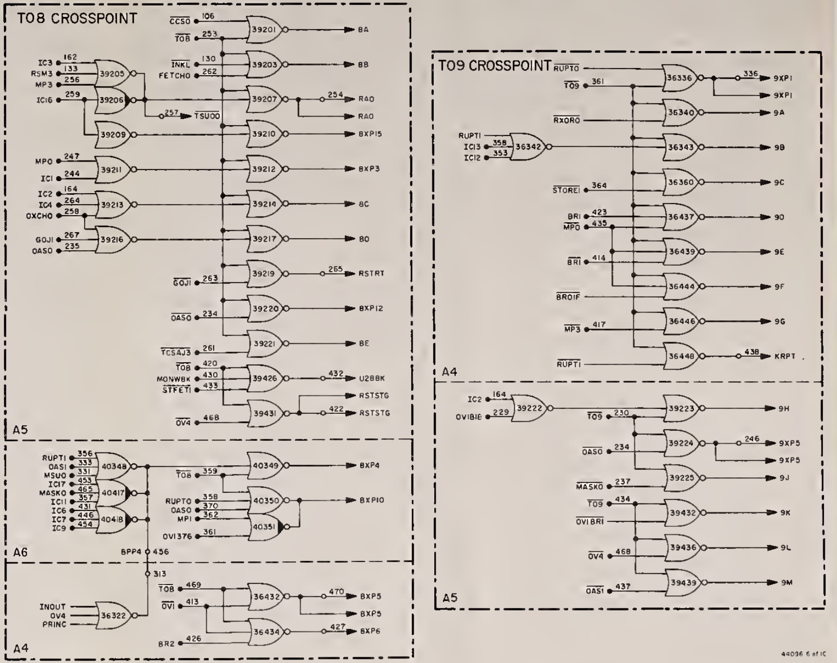

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Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 6 of 10)

TIO CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
MPOTIO	ST1 TSGN	TIO MPO
IOA	RL	TIO MP3
IOB	ST2 WY	TIO CCSO
IOXP6	CI MONEX	TIO CCSO $\overline{BR2}$
IOXP1	ST1	TIO (IC1 + IC10 + RUPTO)
IOC	RA WY	TIO (OASO + MSUO BR1)
IOXP7	MONEX	TIO (MSUO BR1 + OASO BR1 $\overline{BR2}$)
IOXP8	PONEX	TIO OASO $\overline{BR1}$ BR2
IOD	RU WB	TIO (IC14 + IC2 + DV1)
IOXP10	A2X WY	TIO IC11
IOE	WL	TIO (IC4 + OV4 $\overline{BR1}$ + OAS1 $\overline{AOSO}$ $\overline{BR2}$)
EXT	EXT	TIO NDXXI
IOXP9	RB	TIO (IC6 + OCAO + ADO + CCSO $\overline{BR1}$ $\overline{BR2}$)
IOF	WA	TIO (IC6 + IC7)
IOG	RC	TIO (IC7 + OCSO + SUO + CCSO BR1 $\overline{BR2}$ + OV4 $\overline{BR1}$)
IOXP15	ST1 ST2	TIO MPI

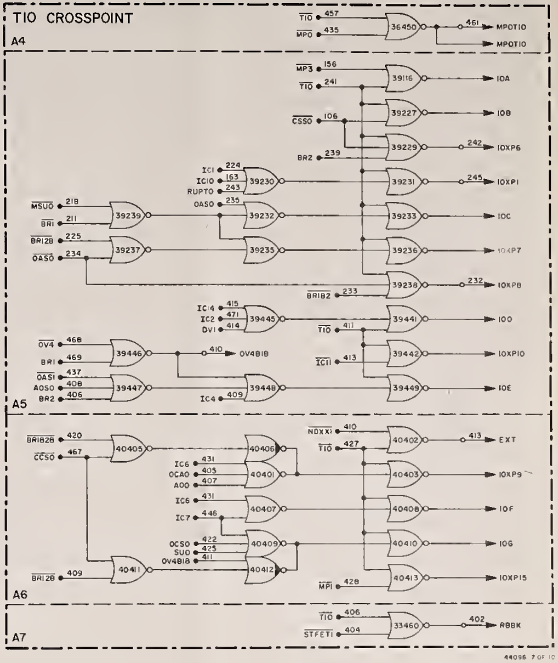
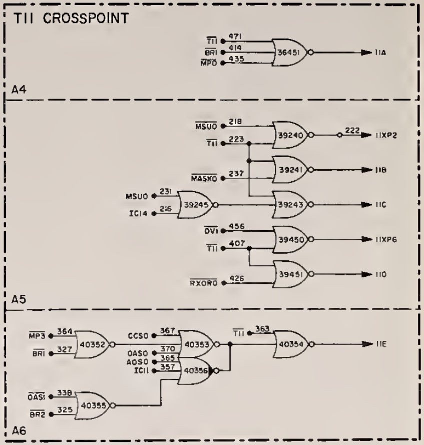


Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 7 of 10)

TI1 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
11A	RIC RB1	T11 MP0 BR1
11XP2	RUS	T11 MSU0
11B	RC	T11 MASK0
11C	WA	T11 (MSU0 + IC14)
11XP6	RL WY0	T11 OV1
11D	RC RG	T11 RXOR0
11E	RY WA	T11 (CCS0 + MP3 BR1 + OAS0 + AOS0 + IC11 + OAS1 BR2)

T12 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
12A	RU	T12 · T12USE OV1



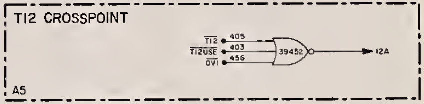


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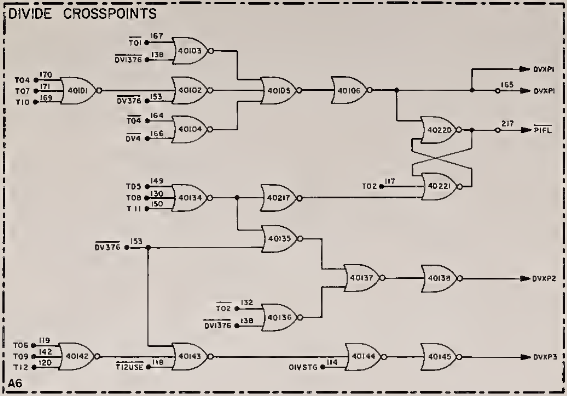
Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 8 of 10)



DIVIDE CROSSPOINTS		
SIGNAL	CONTROL PULSES	EQUATION
DVXP1	A2X L2GD RB WYD	DVI376 T01 + DV376 (T04 + T07 + T10) + DV4 T04
PIFL	PIFL	DVXP1 + $\overline{(T02 + T05 + T08 + T11)}$ PIFL
DVXP2	RG TSGU WL	DVI376 T02 + DV376 (T05 + T08 + T11)
DVXP3	RU WB	DV376 (T06 + T09 + T12) T12USE + DIVSTG

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Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 9 of 10)

MULTIPLY CROSSPOINTS		
SIGNAL	CONTROL PULSES	EQUATION
ZIP	A2X L2GO	2XP7 + MP1 (T01 + T03 + T05 + T07 + T09 + T11)
MPXP1	WY	ZIP $(\overline{\overline{L15A} \cdot L02A \cdot \overline{L01}}) (\overline{L15A \cdot \overline{L02A} \cdot L01})$
MPXP2	WYD	ZIP $(\overline{L15A} \cdot L02A \cdot \overline{L01} + L15A \cdot \overline{L02A} \cdot L01)$
MCRO	MCRO	ZIP $(L02A \cdot \overline{\overline{L15A} \cdot L02A \cdot \overline{L01}})$
ZIPCI	RC CI	ZIP $L02A \cdot (\overline{\overline{L15A} \cdot L02A \cdot \overline{L01}}) \cdot (\overline{L15A \cdot L02A \cdot L01})$
MPXP3	RB	ZIP $(\overline{L02A} + \overline{L15A} \cdot L02A \cdot \overline{L01} + \overline{\overline{L15A} \cdot \overline{L02A} \cdot \overline{L01}})$
ZAP	G2LS RU WALS	MP1 (T02 + T04 + T06 + T08 + T10) + MP3 (T01 + T03)

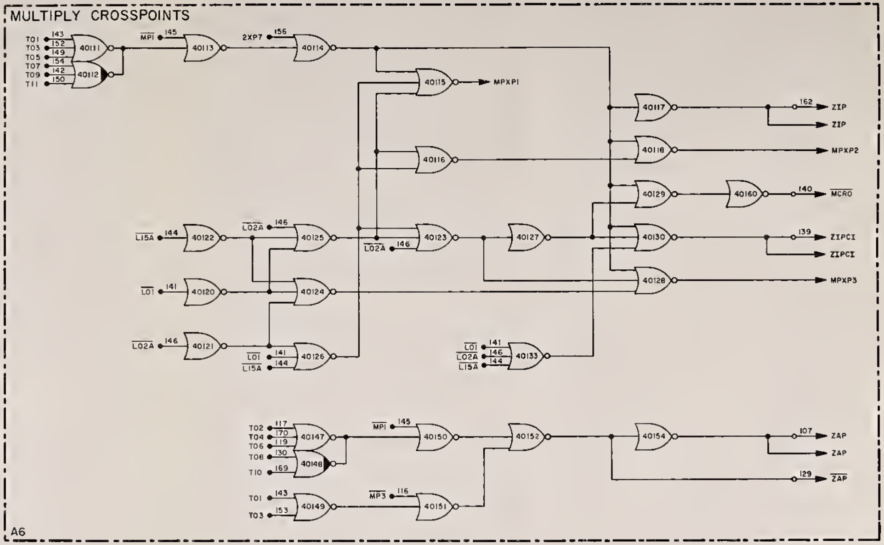

Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 10 of 10)

At time pulse T05, crosspoint pulses 5G and 5J are produced from commands CCS0 and IC12, respectively. Crosspoint pulse 5G may also be produced from command PARTC or PINC. Crosspoint pulse 5G produces control pulses RG, TMZ, TPZG, and TSGN. Control pulse RG places the content of register G onto the write lines. The branch flip-flops are set to the 00 state if register G and the write lines contain a positive quantity. Control pulse TSGN resets the branch 1 flip-flop and control pulses TMZ and TPZG reset the branch 2 flip-flop. Branch state 01 is established if register G contains a plus zero. Control pulse TSGN resets the branch 1 flip-flop and control pulse TPZG, in conjunction with the decoded output of register G, sets the branch 2 flip-flop. Branch state 10 is established if the write lines contain a negative quantity other than minus zero. Control pulse TSGN, in conjunction with signal WL16, sets the branch 1 flip-flop and control pulses TPZG and TMZ reset the branch 2 flip-flop. Finally, state 11 is established when the write lines contain minus zero. The branch 1 flip-flop is set by control pulse TSGN and signal WL16. The branch 2 flip-flop is set by signals WL16 through WL01 and control pulse TMZ. The output of the branch flip-flops are decoded into various branch command signals that are used for producing crosspoint pulses.

Crosspoint pulse 5J is converted into control pulses RG and WB. Control pulse RG is also produced from crosspoint pulse 5G, thus making one RG control pulse redundant. Control pulse RG places the content of register G onto the write lines. Control pulse WB transfers the write line information into register B. Crosspoint pulse 5J can only be produced by time pulse signal T05 and instruction command signal IC12. No crosspoint pulses are produced at time pulse T06 of subinstruction CCS0.

At time pulse T07, the state of the branch flip-flops determines what crosspoint pulses are produced. The control pulses at time pulse T07 will add plus zero, one, two, or three to the address c(Z) contained in register Z if the branch flip-flops are in state 00, 01, 10, or 11, respectively. Crosspoint pulse 7D is produced by signals T07 and CCS0 and is not dependent on the state of the branch flip-flops. Signal 7D is converted into control pulses RZ and WY12 which copy the twelve (12) low order bits of register Z into the adder register Y. Control pulse WY12 also clears adder register X and the carry flip-flop. If the branch flip-flops are in the 00 state, no further action occurs at time pulse T07 and the adder gates U contain $c(Z) + 0 = c(Z)$. If the branch 2 flip-flop is set as it is for states 01 and 11, crosspoint pulse 7XP4 is produced. Signal 7XP4 is produced by time pulse T07, subinstruction command CCS0, and branch signal BR2. Crosspoint pulse 7XP4 is then converted into control pulse PONEX which sets bit 1 of adder register X. If the branch flip-flops are in the 01 state, no further action occurs at time pulse T07. As a result, the adder gates U contain $c(Z) + 1$. If the branch flip-flops are in the 11 state, crosspoint pulse PTWOX is produced by signals T07, CCS0, and BR1. Signal PTWOX, which is used as the control pulse, sets bit 2 of register X. Since register X now contains octal three from the action of control pulses PONEX and PTWOX, the adder output gates contain $c(Z) + 3$. Had the branch flip-flops been set to state 10, only control pulse PTWOX would be produced and the output gates U would contain $c(Z) + 2$.

At time pulse T08, crosspoint pulse 8XP10 is produced and converted to control pulse WS. Signal 8XP10 is produced involuntarily every T08 time pulse except when inhibited by subinstruction commands RUPT0, DAS0, or MP1 or instruction command DV1376. Control pulse WS is used for copying an address into register S. The address usually comes from register Z; however, it may also come from the priority control, peripheral equipment, register B or adder gates. Signals T08 and CCS0 also produce crosspoint pulse 8A which is converted to control pulses RU and WZ. Control pulses RU, WZ, and WS enter the content of the adder gates U into registers Z and S. At time pulse T09, crosspoint pulse 9B is produced from signals T09 and IC12 and converted into control pulses RB and WB. Crosspoint pulse 9B may also be produced by signal RUPT1 or IC13. Control pulses RB and WB copy the content of register B into register G. This is the quantity that was originally taken out of erasable memory at time pulse T04 and entered into register G. The content of register G is returned to its erasable memory location at time pulse T10. This action does not destroy the same data contained in register B.

Also at time pulse T10, control pulses WY and ST2 are produced from crosspoint pulse 10B. Control pulse ST2 sets the primary level flip-flops of the stage counter to 010 in preparation for subinstruction STD2. Control pulse WY clears register X and enters the content of the write lines into register Y. If the branch flip-flops are set to state 01 or 11, no additional crosspoint and control pulses are produced. As a result, the adder gates U contain plus zero. If the branch 2 flip-flop is reset, as it is for states 00 and 10, crosspoint pulse 10XP6 is produced and converted to control pulses CI and MONEX. Control pulse CI sets the carry flip-flop and control pulse MONEX sets register X to minus one or octal 177776. Crosspoint pulse 10XP6 is produced by signals T10 and CCS0, when signal BR2 is not present. If the quantity c(E) taken from erasable memory is positive, the branch flip-flops will be in the 00 state. Crosspoint pulse 10XP9 will produce control pulse RB which in turn will copy the positive quantity in register B onto the write lines. Control pulse WY will then enter c(E) into register Y. The quantity c(E) in register Y, minus one in register X, and a carry bit results in c(E) -1 at the output gates U. If the original quantity in erasable memory was negative c(E), the branch flip-flops will be in state 10, and crosspoint pulse 10G will produce control pulse RC. Control pulse RC converts the negative quantity c(E) in register B into the equivalent positive quantity c(E) by gating the complement output of register B onto the write lines. As a result, the same net results are obtained as with a positive quantity, namely c(E) -1 at output gates U. Crosspoint pulse 10G is also produced by commands IC7, DCS0, SU0, and a particular branch condition during DV4.

The last action of subinstruction CCS0 occurs at time pulse T11 during which crosspoint pulse 11E is produced and converted into control pulses RU and WA. These control pulses cause the content of adder gates U to be copied into register A. Crosspoint pulse 11E is also produced from signals DAS0, ADS0, IC11, and particular branch conditions of MP3 and DAS1. Subinstruction CCS0 is followed by subinstruction STD2.

Special attention is given to the divide instruction because the crosspoint circuit, which produces pulses DVXP1 through DVXP3 and PIFL, differs from the T01 through T12 crosspoint circuits (figure 4-134). The crosspoint and control pulses for subinstructions DV0, DV1, DV3, DV7, DV6, and DV4 are listed in tables 4-XIII through 4-XVII.

Table 4-XIII. Subinstruction DV0

Time	BR1 and BR2	Involuntary		DV0		DIV	
		XP	CP	XP	CP	XP	CP
1				1XP10	RA TMZ TSGN WB		
2	XX	△1				DVST	
2	0X			2XP5	RC TMZ WA		
3	△2	DIVSTG (DVXP3)	RU WB				

△1 Crosspoint pulse 2B is inhibited by command DV0.

△2 Crosspoint pulse DIVSTG is involuntary during the DV instruction. Crosspoint pulse DIVSTG also produces signal DVXP3 which is converted into control pulses RU and WB.

Table 4-XIV. Subinstruction DV1, Part 1

Time	BR1 and BR2	Involuntary		DV1	
		XP	CP	XP	CP
4	XX			4K 4L	RL WB
4	X1			4D	TSGN
5	XX			B15X	WY
5	0X			5XP19	RB
5	1X			5R Z16	RC
6				6XP5	RU TOV WL
7				7A	RSC TSGN
				7F	RG WB
8	XX			8XP5	RA WY
8	X0	[1]		8XP6	PONEX
9	0X			9H	RB WA
9	1X			9K	RC WA Z15
10				10D	RU WB
11				11XP6	RL WYD
12				12A	RU WL

[1] Crosspoint pulse 8XP10 is inhibited by command DV1.

Table 4-XV. Subinstructions DV3, DV7, and DV6, Part 1

Time	BR1 and BR2	Involuntary		DV376	
		XP	CP	XP	CP
4				DVXP1	A2X L2GD RB WYD
				PIFL	
5	XX			DVXP2	RG TSGU WL
5	0X				CLXC
5	1X				RB1F
6				DVXP3	RU WB
7				DVXP1	A2X L2GD RB WYD
				PIFL	
8	XX	△1		DVXP2	RG TSGU WL
8	0X				CLXC
8	1X				RB1F
9				DVXP3	RU WB
10				DVXP1	A2X L2GD RB WYD
				PIFL	
11	XX			DVXP2	RG TSGU WL
11	0X				CLXC
11	1X				RB1F
12				DVXP3	RU WB

△1 Crosspoint pulse 8XP10 is inhibited by command DV1376.

Table 4-XVI. Subinstructions DV1, DV3, DV7, and DV6, Part 2

Time	BR1 and BR2	Involuntary		DV1376		DIV	
		XP	CP	XP	CP	XP	CP
1				DVXP1 PIFL	A2X L2GD RB WYD		
2	XX	[1]		DVXP2	RG WL TSGU	DVST	
2	0X				CLXC		
2	1X				RB1F		
3	[2]	DIVSTG (DVXP3)	RU WB				

[1] Crosspoint pulse 8XP10 is inhibited by command DV1376.

[2] Crosspoint pulse DIVSTG produces signal DVXP3 which is converted into control pulses RU and WB.

Table 4-XVII. Subinstruction DV4

Time	BR1 and BR2	Involuntary		DV4	
		XP	CP	XP	CP
4				DVXP1 PIFL	A2X L2GD RB WYD
5	XX			5XP28 5S	RG TSGU WB WA
5	0X				CLXC
5	1X				RB1F
6				6XP7	RZ TOV
7	X1			7XP7	RC WA
7	1X			7XP7	RC WA
8		8XP10	WS	RSTSTG 8XP4	TSGN RZ ST2
9				9L	RU WB WL
10	0X			10E 10G	WL RC

The crosspoint and control pulses for subinstruction DV0 and part 1 of subinstruction DV1 (tables 4-XIII and 4-XIV) are produced in the conventional manner by the T01 through T12 crosspoint circuits. The crosspoint pulses listed in tables 4-XV and 4-XVI and some of those listed in table 4-XVII are produced by the divide crosspoint circuit. This circuit is controlled by instruction commands DV1376 and DV376; subinstruction command DV4; signals DIVSTG and T12USE; and all time pulses except T03. Instruction command DV1376 is used to produce crosspoint pulse DVXP1 at time pulse T01. Crosspoint pulse DVXP1 is also produced at time pulse T04, T07, and T10 by instruction command DV376 and at time pulse T04 by subinstruction command DV4. Crosspoint pulse DVXP1 is converted into control pulses A2X, L2GD, RB, and WYD, by the control pulse gates. Control pulses CLXC and RB1F are discussed in detail in the branch control circuit description.

Signal DVXP1 is also applied to the set side of the PIFL flip-flop. Signals DVXP1 and PIFL occur simultaneously since the reset side of the PIFL flip-flop is pulsed at time pulses T02, T05, T08, and T11.

Crosspoint pulse DVXP2 is produced at time pulse T02 by instruction command DV1376 and at time pulses T05, T08, and T11 by instruction command DV376. This signal is converted into control pulses RG, TSGU, and WL.

Control pulse DIVSTG occurs at time pulse T03 of the divide subinstructions and produces crosspoint pulse DVXP3. Signal DVXP3 is also produced at time pulses T06, T09, and T12 when signals DV376 and T12USE are present. Signal T12USE is a flip-flop signal produced by the stage counter and decoder circuit. Crosspoint pulse DVXP3 is converted into control pulses RU and WB.

The multiply instruction also requires special consideration because the multiply crosspoint circuit differs from the conventional T01 through T12 crosspoint circuits. The multiply crosspoint circuit produces signals ZIP, ZAP, MPXP1, MPXP2, MPXP3, MCRO, and ZIPCI, as shown in figure 4-134 and listed in tables 4-XVIII through 4-XXI. Crosspoint pulse ZIP is converted into control pulses A2X and L2GD and is produced at time pulses T01, T03, T05, T07, T09, and T11 of subinstruction MP1. It is also produced by crosspoint pulse 2XP7 which occurs at time pulse T02 during subinstruction MP3.

Table 4-XVIII. Subinstruction MP0

Time	BR1 and BR2	Involuntary		MP0		IC14	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
3				3C 3F	TSGN RA WB		
4	0X			4B	RB WL		
4	1X			4C	RC WL		
7				TSGN2		7F	RG WB
8		8XP10	WS	8XP3	RZ		
9	0X			9D	RB WY		
9	1X			9E	RC WY		
9	01			9F	CI		
9	10			9F	CI		
10		[1]		MP0T10	ST1 TSGN	10D	RU WB
				10A	RL		
11	XX					11C	WA
11	1X			11A	R1C RB1		

[1] Control pulse NEACON is produced in the adder at time period T10 and inhibits end around carry.

Table 4-XIX. Subinstruction MP1

Time	BR1 and BR2	Involuntary		MP1	
		XP	CP	XP	CP
1			[2]	ZIP	A2X L2GD
2		[1]		ZAP	G2LS RU WALS
3				ZIP	A2X L2GD
4				ZAP	G2LS RU WALS
5				ZIP	A2X L2GD
6				ZAP	G2LS RU WALS
7				ZIP	A2X L2GD
8				ZAP	G2LS RU WALS
9				ZIP	A2X L2GD
10				ZAP	G2LS RU WALS
				10XP15	ST1 ST2
11				ZIP	A2X L2GD

[1] Crosspoint pulses 2B and 8XP10 are inhibited by command MP1.

[2] See table 4-XXI for additional crosspoint pulses produced by ZIP.

Table 4-XX. Subinstruction MP3

Time	BR1 and BR2	Involuntary		MP3	
		XP	CP	XP	CP
1				ZAP	G2LS RU WALS
2		[1]	[2]	ZIP	A2X L2GD
3				ZAP	G2LS RU WALS
4				4E	RSC WG
5				5P	RZ WY12 CI
6		[3]		TL15 6D	RU WZ
7	1X			7XP19	A2X RB WY
8		8XP10	WS	RAD	WB
9				9G	RA
10				10A	RL
11	1X			11E	RU WA

[1] Crosspoint pulse 2B is inhibited by command MP3.

[2] See table 4-XXI for additional crosspoint pulses produced by ZIP.

[3] Control pulse NEACOF is produced in the adder at time period T06 and permits end around carry.

Table 4-XXI. Crosspoint Pulse ZIP

c(L)	ZIP	
15, 2, 1	XP	CP
000	MPXP1	WY
001	MPXP1	WY
	MPXP3	RB
010	MPXP2	WYD
	MPXP3	RB
011	MPXP1	WY
	ZIPCI	RC
		CI
	MCR0	
100	MPXP1	WY
	MPXP3	RB
101	MPXP2	WYD
	MPXP3	RB
110	MPXP1	WY
	ZIPCI	RC
		CI
	MCR0	
111	MPXP1	WY
	MCR0	

Crosspoint pulses MPXP1 through MPXP3, MCRO, and ZIPCI are dependent on the state of bits 15, 2, and 1 of register L and are produced in conjunction with crosspoint pulse ZIP. Table 4-XXI lists the crosspoint and control pulses produced by signal ZIP for all possible states of these bits. Crosspoint pulse MPXP1 is produced and converted into control pulse WY for all states except 010 and 101. During states 010 and 101, crosspoint pulse MPXP2 is produced instead of MPXP1 and converted into control pulse WYD. Control pulse RB is produced from crosspoint pulse MPXP3 during states 001, 010, 100, and 101 whereas control pulses RC and CI are produced from ZIPCI during states 011 and 110. In addition, crosspoint pulse MCRO is produced during states 011, 110, and 111 and used directly as a control pulse.

Crosspoint pulse ZAP is produced and converted into control pulses G2LS, RU, and WALS at time pulses T02, T04, T06, T08, and T10 of subinstruction MP1. It is also produced at time pulses T01 and T03, during subinstruction MP3.

During the multiply instruction, the adder is switched to perform arithmetic in the two's complement system. Switching is accomplished by signal NEACON which occurs at time pulse T10 of subinstruction MP0. Signal NEACON sets a flip-flop (part of the adder) which inhibits end around carry until it is reset by signal NEACOF at time pulse T06 of subinstruction MP3.

Tables 4-XXII through 4-LXXIV list the crosspoint and control pulses produced for the remaining subinstructions.

4-5.4.11 Control Pulse Gates. The control pulse gates (figure 4-135) convert crosspoint pulses into control pulses. For example, control pulse NISQ is produced by crosspoint pulse 2C, 2XP7, or 8XP15. A single crosspoint pulse may produce several control pulses. For example, crosspoint pulse 2XP5 produces control pulses RC, TMZ, and WA. Two control pulses, CLXC and RB1F, produced from control pulse TSGU, signal PHS4, and a branch signal, occur during the divide instruction. Only one is produced at a time. Control pulse CLXC is produced when the branch flip-flops are in the 0X state and control pulse RB1F is produced during the 1X state. Control pulse TSGU is produced by crosspoint pulse 5XP28 or DVXP2. Table 4-LXXV lists all of the control pulses produced by the control pulse gates and other circuits.

Table 4-XXII. Subinstruction STD2

Time	BR1 and BR2	Involuntary		STD2		IC3	
		XP	CP	XP	CP	XP	CP
1				1C	RZ	1A	WY12 CI
2		2B	RSC WG			2C	NISQ
6						6D	RU WZ
8		8XP10	WS			RAD	WB

Table 4-XXIII. Subinstruction TC0

Time	BR1 and BR2	Involuntary		TC0		IC3	
		XP	CP	XP	CP	XP	CP
1				1D	RB	1A	WY12 CI
2		2B	RSC WG			2C	NISQ
3				3XP6	RZ WQ		
6						6D	RU WZ
8		8XP10	WS			RAD	WB

Table 4-XXIV. Subinstruction TCF0

Time	BR1 and BR2	Involuntary		TCF0		IC3	
		XP	CP	XP	CP	XP	CP
1				1D	RB	1A	WY12 CI
2		2B	RSC WG			2C	NISQ
6						6D	RU WZ
8		8XP10	WS			RAD	WB

Table 4-XXV. Subinstruction TCSAJ3

Time	BR1 and BR2	Involuntary		TCSAJ3	
		XP	CP	XP	CP
2		2B	RSC WG		
8		8XP10	WS	8E	WZ ST2

Table 4-XXVI. Subinstruction GOJ1

Time	BR1 and BR2	Involuntary		GOJ1	
		XP	CP	XP	CP
2		2B	RSC WG		
8		8XP10	WS	8D RSTRT	WB

Table 4-XXVII. Subinstruction DAS0

Time	BR1 and BR2	Involuntary		DAS0		IC10	
		XP	CP	XP	CP	XP	CP
1				RL10BB	WS	1A 1B	CI WY12 MONEX
2		2B	RSC WG				
3				3F	RA WB		
4				4H	RL WA		
5				5XP12	RU WL		
6				6B	A2X RG WY		
7				7B 7G	RB WA		
8		△1		8D 8XP12	WB RL		
9				9XP5	RU TOV WG WSC		
10	XX			10C	RA WY	10XP1	ST1
10	01			10XP8	PONEX		
10	10			10XP7	MONEX		
11				11E	RU WA		

△1 Crosspoint pulse 8XP10 is inhibited by command signal DAS0.

Table 4-XXVIII. Subinstruction DAS1

Time	BR1 and BR2	Involuntary		DAS1	
		XP	CP	XP	CP
1				RL10BB	WS
2		2B	RSC WG		
5				5K 5L	RG A2X WY
6				6XP8	RU TOV WG WSC
7	XX			7G	WA
7	01			7XP10	RB1
7	10			7XP11	R1C
8		8XP10	WS	8XP4	RZ ST2
9				9M	RC TMZ
10	X0			10E	WL
11	01			11E	RU WA

Table 4-XXIX. Subinstruction LXCH0

Time	BR1 and BR2	Involuntary		IC8		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3G	RL WB		
5				5XP13	RG WL		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XXX. Subinstruction INCR0

Time	BR1 and BR2	Involuntary		INCR0		PRINC	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5G 5L	RG TMZ TPZG TSGN WY
6				6XP10	PONEX		
7						7H WOVR	RU WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XXXI. Subinstruction ADS0

Time	BR1 and BR2	Involuntary		ADS0		DAS1	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5K	RG A2X
						5L	WY
6						6XP8	RU TOV WG WSC
7	XX					7G	WA
7	01					7XP10	RB1
7	10					7XP11	R1C
8		8XP10	WS			8XP4	RZ ST2
9						9M	RC TMZ
11	XX			11E	RU WA		
11	01					11E	RU WA

Table 4-XXXII. Subinstructions CA0 and DCA1

Time	BR1 and BR2	Involuntary		IC6		IC13	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
7						7F	RG WB
8		8XP10	WS	8XP4	RZ ST2		
9						9B	RB WG
10				10XP9 10F	RB WA		

Table 4-XXXIII. Subinstructions CS0 and DCS1

Time	BR1 and BR2	Involuntary		IC7		IC13	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
7						7F	RG WB
8		8XP10	WS	8XP4	RZ ST2		
9						9B	RB WG
10				10G 10F	RC WA		

Table 4-XXXIV. Subinstruction NDX0

Time	BR1 and BR2	Involuntary		NDX0		IC1		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
5				TRSM					
7								7F	RG WB
8		8XP10	WS			8XP3	RZ		
9								9B	RB WG
10						10XP1	ST1		

Table 4-XXXV. Subinstruction RSM3

Time	BR1 and BR2	Involuntary		RSM3	
		XP	CP	XP	CP
1				R15	
2		2B	RSC WG	2C	NISQ
5				5XP4	RG WZ
6				6A	RB WG
8		8XP10	WS	RAD	WB

Table 4-XXXVI. Subinstruction NDX1

Time	BR1 and BR2	Involuntary		IC2	
		XP	CP	XP	CP
1				1A 1C	WY12 CI RZ
2		2B	RSC WG	2C	NISQ
3				3XP5	RB WZ
4				4F 4L	RA WB
5				5H 5S	RZ WA
6				6D	RU WZ
7				7C	A2X RG WY
8		8XP10	WS	8C	RU
9				9H	RB WA
10				10D	RU WB

Table 4-XXXVII. Subinstruction XCH0

Time	BR1 and BR2	Involuntary		IC5		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3F	RA WB		
5				5Q 5S	RG WA		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XXXVIII. Subinstruction DXCH0

Time	BR1 and BR2	Involuntary		DXCH0		IC8		IC10	
		XP	CP	XP	CP	XP	CP	XP	CP
1				RL10BB	WS			1A 1B	WY12 CI MONEX
2		2B	RSC WG						
3						3G	RL WB		
5						5XP13	RG WL		
7				7J	RB WG WSC				
8		8XP10	WS	8C 8D	RU WB				
10								10XP1	ST1

Table 4-XXXIX. Subinstruction DXCH1

Time	BR1 and BR2	Involuntary		IC5		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3F	RA WB		
5				5Q 5S	RG WA		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XL. Subinstruction TS0

Time	BR1 and BR2	Involuntary		TS0		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3XP2 3F	TOV RA WB		
4	XX			4XP5	RZ WY12		
4	01			4A	CI L16		
4	10			4A	CI L16		
5	01			5E 5S	RB1 WA		
5	10			5F 5S	R1C WA		
6				6D	RU WZ		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLI. Subinstruction AD0

Time	BR1 and BR2	Involuntary		AD0		IC11		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
7								7F	RG WB
8		8XP10	WS			8XP4	RZ ST2		
9								9B	RB WG
10				10XP9	RB	10XP10	A2X WY		
11						11E	RU WA		

Table 4-XLII. Subinstruction MASK0

Time	BR1 and BR2	Involuntary		MASK0		IC14	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
3				3F	RA WB		
4				4J	RC WA		
7						7F	RG WB
8		8XP10	WS	8XP4	RZ ST2		
9				9J	RA RC WY		
10						10D	RU WB
11				11B	RC	11C	WA

Table 4-XLIII. Subinstruction BZF0

Time	BR1 and BR2	Involuntary		IC15		IC16		IC17	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
3				3E	RA TMZ TSGN WG				
4				4G	TPZG				
5	X1	[1]				5N	RB WY12 CI		
6	X1					6D	RU WZ		
8	XX	8XP10	WS						
8	X1					RAD 8XP15	WB NISQ		
8	X0	[2]						8XP4	RZ ST2

[1] Branch condition X1 produces command IC16.

[2] Branch condition X0 produces command IC17.

Table 4-XLIV. Subinstruction MSU0

Time	BR1 and BR2	Involuntary		MSU0		IC12	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5J	RG WB
6				6C	A2X CI RC WY		
7				7XP9	RUS TSGN		
				7G	WA		
8		8XP10	WS	8XP4	RZ ST2		
9						9B	RB WG
10	1X			10C	RA WY		
				10XP7	MONEX		
11				11XP2 11C	RUS WA		

Table 4-XLV. Subinstruction QXCH0

Time	BR1 and BR2	Involuntary		QXCH0		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				RQ	WB		
5				5XP15	RG WQ		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLVI. Subinstruction AUG0

Time	BR1 and BR2	Involuntary		AUG0		PRINC	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5G 5L	RG TMZ TPZG TSGN WY
6	0X			6XP10	PONEX		
6	1X			6E	MONEX		
7						7H WOVR	RU WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLVII. Subinstruction DIM0

Time	BRI and BR2	Involuntary		DIM0		PRINC	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5G	RG TMZ TPZG TSGN
						5L	WY
6	00			6E	MONEX		
6	10			6XP10	PONEX		
7						7H WOVR	RU WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLVIII. Subinstruction DCA0

Time	BR1 and BR2	Involuntary		DCA0		IC4		IC10		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP	XP	CP
1						1D	RB	1A 1B	CI WY12 MONEX		
2		2B	RSC WG								
7										7F	RG WB
8		8XP10	WS			8C	RU				
9										9B	RB WG
10				10XP9	RB	10E	WL	10XP1	ST1		

Table 4-XLIX. Subinstruction DCS0

Time	BR1 and BR2	Involuntary		DCS0		IC4		IC10		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP	XP	CP
1						1D	RB	1A 1B	CI WY12 MONEX		
2		2B	RSC WG								
7										7F	RG WB
8		8XP10	WS			8C	RU				
9										9B	RB WG
10				10G	RC	10E	WL	10XP1	ST1		

Table 4-L. Subinstruction SU0

Time	BR1 and BR2	Involuntary		SU0		IC11		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
7								7F	RG WB
8		8XP10	WS			8XP4	RZ ST2		
9								9B	RB WG
10				10G	RC	10XP10	A2X WY		
11						11E	RU WA		

Table 4-L1. Subinstruction NDXX0

Time	BR1 and BR2	Involuntary		IC1		IC13	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
7						7F	RG WB
8		8XP10	WS	8XP3	RZ		
9						9B	RB WG
10				10XP1	ST1		

Table 4-LII. Subinstruction NDXX1

Time	BR1 and BR2	Involuntary		NDXX1		IC2	
		XP	CP	XP	CP	XP	CP
1						1A 1C	WY12 CI RZ
2		2B	RSC WG			2C	NISQ
3						3XP5	RB WZ
4						4F 4L	RA WB
5						5H 5S	RZ WA
6						6D	RU WZ
7						7C	A2X RG WY
8		8XP10	WS			8C	RU
9						9H	RB WA
10				EXT		10D	RU WB

Table 4-LIII. Subinstruction BZMF0

Time	BR1 and BR2	Involuntary		IC15		IC16		IC17	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
3				3E	RA TMZ TSGN WG				
4				4G	TPZG				
5	X1	△1				5N	RB WY12 CI		
5	1X					5N	RB WY12 CI		
6	X1					6D	RU WZ		
6	1X					6D	RU WZ		
8	X1					RAD 8XP15	WB NISQ		
8	1X					RAD 8XP15	WB NISQ		
8	00	△2						8XP4	RZ ST2
8	XX	8XP10	WS						

△1 Branch condition X1 or 1X produces command IC16.

△2 Branch condition 00 produces command IC17.

Table 4-LIV. Subinstruction READ0

Time	BR1 and BR2	Involuntary		READ0		INOUT	
		XP	CP	XP	CP	XP	CP
1					RL10BB	WS	
2		△1			2XP3	RA WB	
3					3D	WY	
4					4XP11 4L	RCH WB	
5				5A 5S	RB WA	△2	
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

△2 Crosspoint pulse 5XP11 is inhibited by command READ0.

Table 4-LV. Subinstruction WRITE0

Time	BR1 and BR2	Involuntary		WRITE0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1		2A	WG	2XP3	RA WB
3						3D	WY
4						4XP11 4L	RCH WB
5				5B	RA WCH	△2	
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

△2 Crosspoint pulse 5XP11 is inhibited by command WRITE0.

Table 4-LVI. Subinstruction RAND0

Time	BR1 and BR2	Involuntary		RAND0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1				2XP3	RA WB
3				3B	RC	3D	WY
4						4XP11 4L	RCH WB
5				5R	RC	5XP11	RU WA
6						6XP2	RA WB
7				7XP7	RC WA		
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LVII. Subinstruction WANDO

Time	BR1 and BR2	Involuntary		WANDO		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1				2XP3	RA WB
3				3B	RC	3D	WY
4						4XP11 4L	RCH WB
5				5R	RC	5XP11	RU WA
6						6XP2	RA WB
7				7XP7 7XP14	RC WA WCH		
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LVIII. Subinstruction ROR0

Time	BR1 and BR2	Involuntary		ROR0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1				2XP3	RA WB
3				3A	RB	3D	WY
4						4XP11 4L	RCH WB
5				5XP19	RB	5XP11	RU WA
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LIX. Subinstruction WOR0

Time	BR1 and BR2	Involuntary		WOR0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1				2XP3	RA WB
3				3A	RB	3D	WY
4						4XP11	RCH WB
5				5C 5XP19	WCH RB	5XP11	RU WA
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LX. Subinstruction RXOR0

Time	BR1 and BR2	Involuntary		RXOR0		INOUT		IC14	
		XP	CP	XP	CP	XP	CP	XP	CP
1						RL10BB	WS		
2		△1				2XP3	RA WB		
3				3XP7	RC RCH	3D	WY		
4						4XP11 4L	RCH WB		
5				5D	RA RC WG	△2			
7								7F	RG WB
8		8XP10	WS			8XP4	RZ ST2		
9				9A	RC WG				
10								10D	RU WB
11				11D	RC RG			11C	WA

△1 Crosspoint pulse 2B is inhibited by command INOUT.

△2 Crosspoint pulses 5XP11 and 6XP2 are inhibited by command RXOR0.

Table 4-LXI. Subinstruction RUPT0

Time	BR1 and BR2	Involuntary		RUPT0	
		XP	CP	XP	CP
1				R15	WS
2		2B	RSC WG		
9		△1		9XP1	RZ WG
10				10XP1	ST1

△1 Crosspoint pulse 8XP10 is inhibited by command RUPT0.

Table 4-LXII. Subinstruction RUPT1

Time	BR1 and BR2	Involuntary		RUPT1	
		XP	CP	XP	CP
1				R15 RB2	WS
2		2B	RSC WG		
3				RRPA	WZ
8		8XP10	WS	8XP4	RZ ST2
9				9B KRPT	RB WG

Table 4-LXIII. Subinstruction PINC

Time	BR1 and BR2	Involuntary		PINC		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G	RG TMZ TPZG TSGN		
						5L	WY		
6				6XP10	PONEX				
7				7H	RU			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXIV. Subinstruction MINC

Time	BR1 and BR2	Involuntary		MINC		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G	RG TMZ TPZG TSGN		
						6L	WY		
6				6E	MONEX				
7				7H	RU			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXV. Subinstruction PCDU

Time	BR1 and BR2	Involuntary		PCDU		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6				6XP12	CI				
7				7XP15	RUS			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXVI. Subinstruction MCDU

Time	BR1 and BR2	Involuntary		MCDU		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6				6E 6XP12	MONEX CI				
7				7XP15	RUS			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXVII. Subinstruction DINC

Time	BR1 and BR2	Involuntary		DINC		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6	00		△1	POUT 6E	MONEX				
6	10			MOUT 6XP10	PONEX				
6	X1			ZOUT					
7				7H	RU			WOVR	WG WSC
8		8XP10	WS					8B	RB

△1 Crosspoint pulses POUT, MOUT, and ZOUT are three (3) microseconds long, starting at time period T06 and ending with time period T08.

Table 4-LXVIII. Subinstruction SHINC

Time	BR1 and BR2	Involuntary		SHIFT		INKL	
		XP	CP	XP	CP	XP	CP
1						RSCT	WS
2		2B	RSC WG				
5				5XP9	RG TSGN WYD		
7						WOVR	WG WSC
8		8XP10	WS			8B	RB

Table 4-LXIX. Subinstruction SHANC

Time	BR1 and BR2	Involuntary		SHANC		SHIFT		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5				5M	CI	5XP9	RG TSGN WYD		
7								WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXX. Subinstruction INOTRD

Time	BR1 and BR2	Involuntary		CHINC		INKL	
		XP	CP	XP	CP	XP	CP
1				1E	WS	[1]	
2		2B	RSC WG				
5				5XP21	RCH		
8		8XP10	WS			8B	RB

[1] Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

Table 4-LXXI. Subinstruction INOTLD

Time	BR1 and BR2	Involuntary		INOTLD		CHINC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1						1E	WS	[1]	
2		2B	RSC WG						
5						5XP21	RCH		
7				7XP14	WCH				
8		8XP10	WS					8B	RB

[1] Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

Table 4-LXXII. Subinstructions FETCH0 and STORE0

Time	BR1 and BR2	Involuntary		FETCH0		MON		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1				R6	WS			△1	
2		2B	RSC WG	2XP8	ST1 WY				
4						4M	WSC		
8		8XP10	WS					△2	

△1 Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

△2 Crosspoint pulse 8B is inhibited by command MON.

Table 4-LXXIII. Subinstruction FETCH1

Time	BR1 and BR2	Involuntary		MON		STFET1		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG	△1				△2	
7						7E	RG		
8		8XP10	WS			U2BBK	△3	8B	RB
10						RBBK			

△1 Crosspoint pulse 4M is inhibited by command FETCH1.

△2 Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

△3 Crosspoint pulse U2BBK may be inhibited by signal MONWBK from the peripheral equipment.

Table 4-LXXIV. Subinstruction STORE1

Time	BR1 and BR2	Involuntary		MON		STFET1		STORE1		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG							[1]	
4				4M	WSC						
7						7E	RG				
8		8XP10	WS			U2BBK	[2]			8B	RB
9								9C	WG		
10						RBBK					

[1] Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

[2] Crosspoint pulse U2BBK may be inhibited by signal MONWBK from the peripheral equipment.

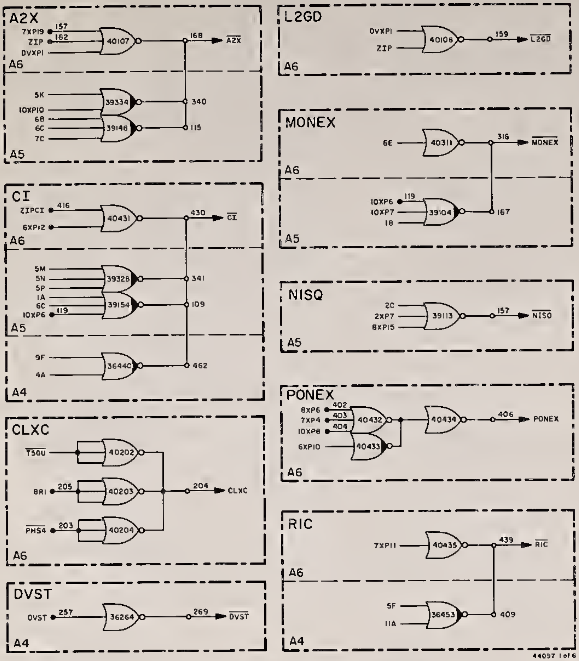

Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 1 of 6)

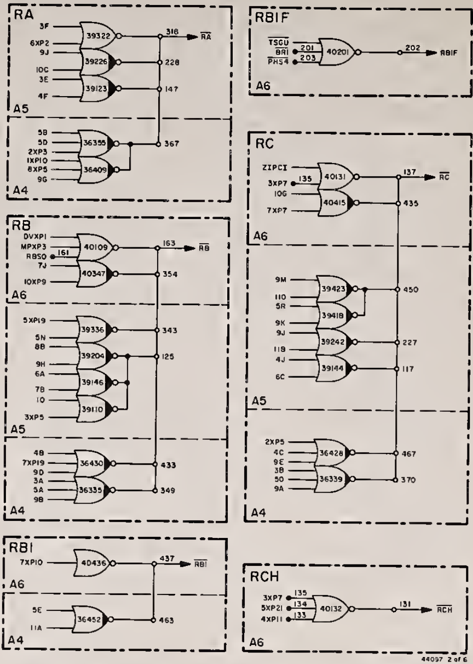

Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 2 of 6)

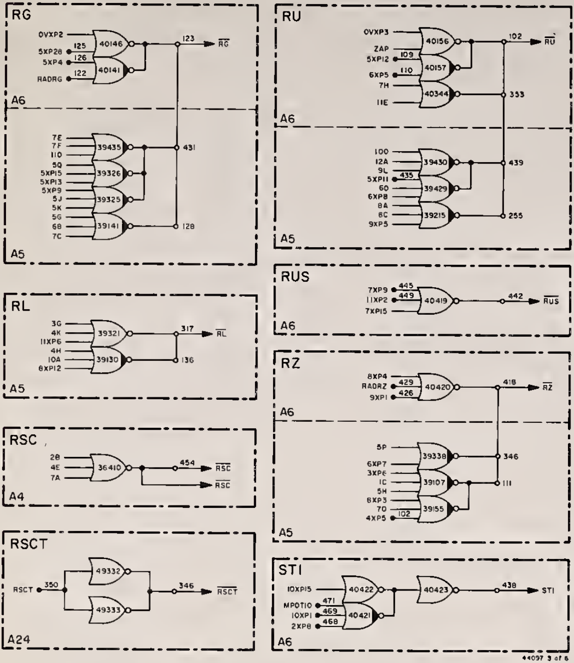

Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 3 of 6)

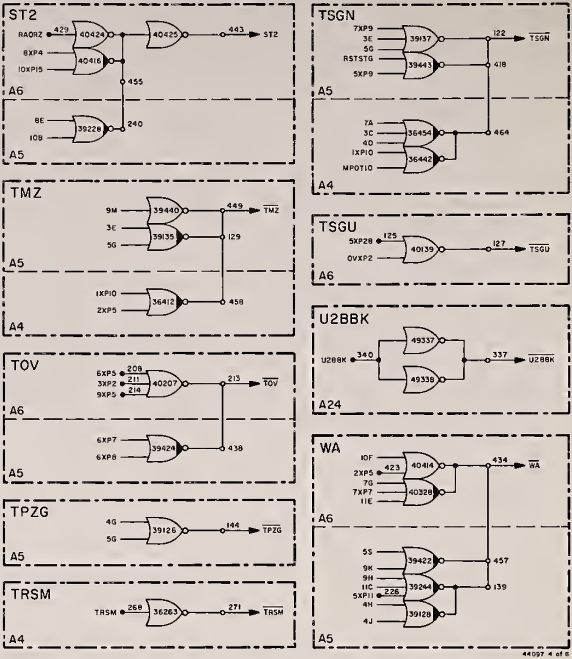

Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 4 of 6)

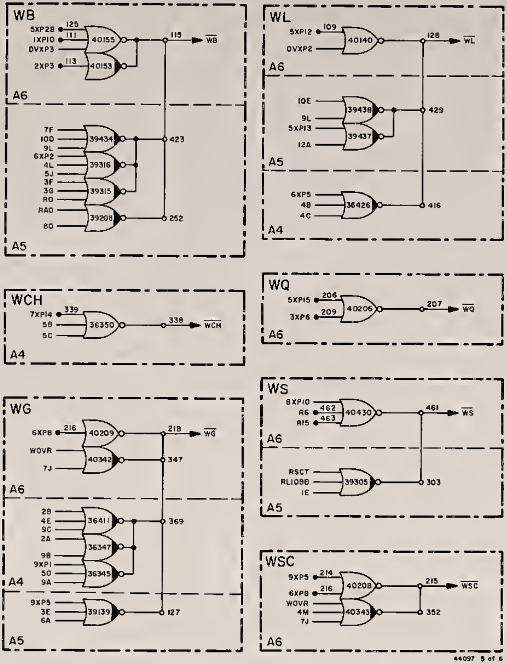

Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 5 of 6)

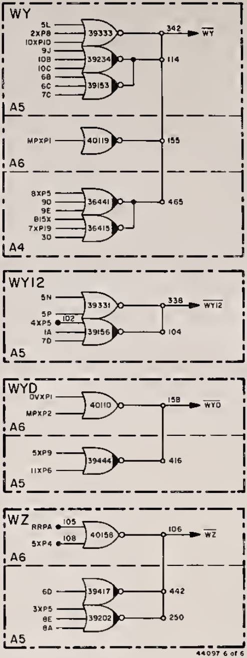

Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 6 of 6)

Table 4-LXXV. Control Pulse Origin

Circuit	Control Pulses	Circuit	Control Pulses
T01 crosspoint	R15	Control pulse gates	NISQ
	RB2	(cont)	PONEX
	RL10BB		R1C
			RA
T03 crosspoint	RRPA		RB
	RQ		RB1
			RB1F
T04 crosspoint	L16 (4A)		RC
			RCH
T05 crosspoint	B15X		RG
	Z16		RL
			RSC
T06 crosspoint	TL15		RSCT
			RU
T07 crosspoint	TSGN2		RUS
	PTWOX		RZ
	WOVR		ST1
			ST2
T08 crosspoint	RAD		TMZ
	RSTRT		TOV
	RSTSTG		TPZG
	Z15 (9K)		TRSM
			TSGN
T09 crosspoint	KRPT		TSGU
			U2BBK
T10 crosspoint	EXT		WA
	RBBK		WB
			WCH
Divide crosspoint	PIFL		WG
			WL
Multiply crosspoint	MCR0		WQ
	ZIP		WS
	ZAP		WSC
			WY
Control pulse gates	A2X		WY12
	C1		WYD
	CLXC		WZ
	DVST		
	L2GD	L service	G2LS
	MONEX		WALS

(Sheet 1 of 2)

Table 4-LXXV. Control Pulse Origin

Circuit	Control Pulses	Circuit	Control Pulses
Channel 14	POUT MOUT ZOUT	Register EB	REB WEB
Adder	NEACOF NEACON	Register FB	RFB WFB WBBK
Register SQ control	WSQ	Stage Counter	DIVSTG (STAGE)

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4-5.4.12 Branch Control. The branch control (figure 4-136) consists of the branch flip-flops, branch decoder, and special instruction flip-flop. The branch flip-flops and decoder control up to four different sets of control pulses at a given time during various subinstructions. The special instruction flip-flop controls two sets of control pulses at a given time depending on whether or not the next instruction to be executed is special instruction RELINT, INHINT, or EXTEND.

The branch 1 flip-flop is used to test the sign bit and the negative overflow bits of any word placed onto the write lines. It also tests bit 15 of register L and bit 16 of the adder. These tests are performed by control pulses TSGN, TOV, TL15, and TSGU, respectively. The test control pulses are similar to write control pulses in that they are used to clear the flip-flop register before or during the write process. As a result, the output of the branch flip-flops cannot be used until the final state is established. Normally all control pulses produced from a branch condition occur one or more time periods after the test control pulses. For example, test control pulse TOV of subinstruction TS0 will establish a new state for the branch flip-flops at time pulse T03. The control pulses resulting from the state of the branch flip-flops are produced at time pulses T04 and T05.

A special case exists for the divide instruction. Control pulse TSGU does not set or reset the branch 1 flip-flop in the normal manner. Bit position 16 of the adder is used as a primary level device with the branch 1 flip-flop being the secondary level device. Control pulse TSGU transfers bit 16 of the adder to the branch 1 flip-flop. If bit 16 is a logic ONE (signals SUMA16 and SUMB16 are present) and the branch 1 flip-flop is already set, no change of state occurs. Signal TSGU is gated by signal PHS3. Therefore, the final state of the branch flip-flop is established 1/4-microsecond before

BRANCH 1 FLIP-FLOP	
SIGNAL	EQUATION
SGUM	SUMA16 SUMB16 TSGU PHS3
A	UNF TOV
B	L15 TL15
C	WL16 TSGN PHS4
D	TSGN PHS3
E	TL15 PHS3
F	$\overline{\text{SUMA16 SUMB16}}$ PHS3 TSGU
G	TOV PHS2
BR1	SGUM + A $\overline{G}$ + B $\overline{E}$ + C + BR1 $\overline{D}$ $\overline{E}$ $\overline{F}$ $\overline{G}$

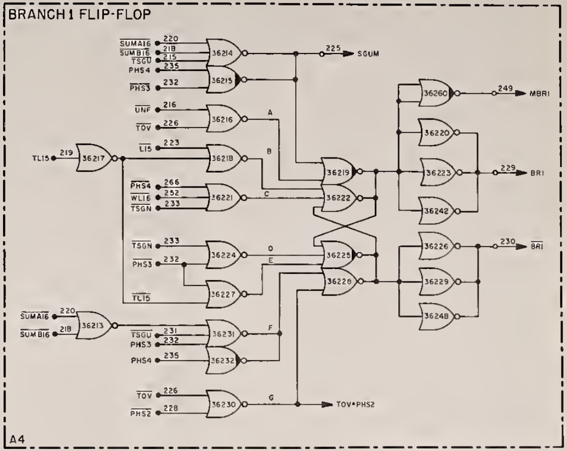
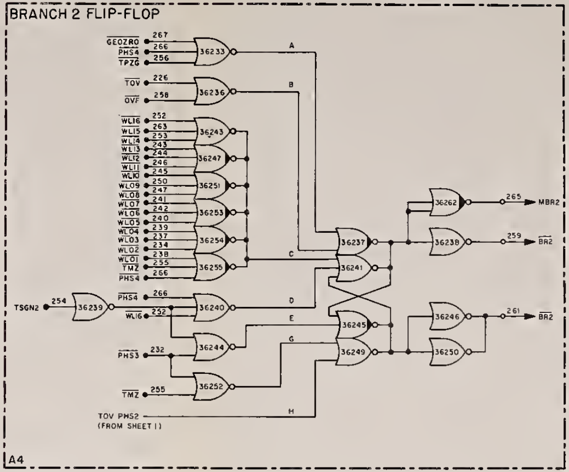
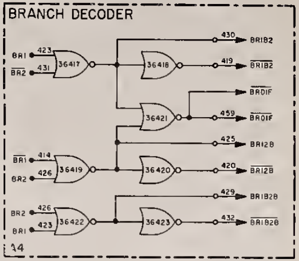


Figure 4-136. Branch Control, Logic Diagram (Sheet 1 of 3)

BRANCH 2 FLIP-FLOP	
SIGNAL	EQUATION
A	GEQZRO TPZG PHS4
B	OVF TOV
C	WL16 WL15 WL14 WL13 WL12 WL11 WL10 WL09 WL08 WL07 WL06 WL05 WL04 WL03 WL02 WL01 TMZ PHS3
D	WL16 TSGN2 PHS4
E	TSGN2 PHS3
G	TMZ PHS3
H	TOV PHS2
BR2	A + B $\bar{H}$ + C + D + BR2 $\bar{E}$ $\bar{F}$ $\bar{G}$ · $\bar{N}$





BRANCH DECODER	
SIGNAL	EQUATION
BR1B2	$\overline{BR1}$ BR2
BRDIF	$\overline{BR1}$ BR2 + BR1 $\overline{BR2}$
BR12B	BR1 $\overline{BR2}$
BR1B2B	$\overline{BR1}$ $\overline{BR2}$

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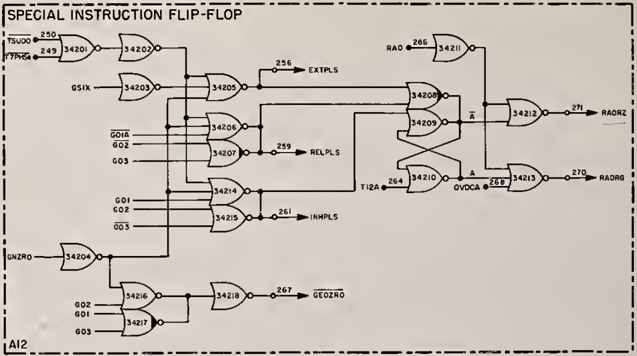
Figure 4-136. Branch Control, Logic Diagram (Sheet 2 of 3)



SPECIAL INSTRUCTION FLIP-FLOP	
SIGNAL	EQUATION
EXTPLS	T7PHS4 TSUD0 GNZR0 GSIX
RELPLS	T2PHS4 TSUD0 GNZR0 $\overline{\text{G03}}$ G02 G01A
INHPLS	T7PHS4 TSUD0 GNZR0 G03 $\overline{\text{G02}}$ $\overline{\text{G01}}$
GEQZR0	GNZR0 $\overline{\text{G03}}$ $\overline{\text{G02}}$ $\overline{\text{G01}}$
A	EXTPLS + RELPLS + INHPLS + A $\overline{\text{T12A}}$
RADRZ	A RAD
RADRG	$\overline{\text{A}}$ RAD

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Figure 4-136. Branch Control, Logic Diagram (Sheet 3 of 3)

control pulse TSGU ends. During this 1/4-microsecond interval, TSGU is gated by signal PHS4 and, in conjunction with the output of the branch 1 flip-flop, produces control pulse CLXC or RB1F. These control pulses are generated by the control pulse gates shown in figure 4-135.

Negative overflow exists when bits 16 and 15 of a word are logic ONE and ZERO, respectively. Negative overflow means that a large negative quantity has been produced in some manner and cannot be processed by the computer because of its limited word length. This condition is monitored during certain operations to prevent faulty computations. When negative overflow exists, a new branch state is established, and a set of control pulses designed to adjust computer operations are produced. The test is accomplished by control pulse TOV. This control pulse is gated by signal PHS2 to first clear the branch 1 and 2 flip-flops. At the same time control pulse TOV tests signal UNF. If signal UNF is present, the branch 1 flip-flop is set. Since the PHS2 signal occurs during the second 1/4-microsecond interval of a time period, the branch 1 flip-flop does not set until the third 1/4-microsecond period.

Control pulse TL15 tests bit 15 of register L. Control pulse TL15 is first gated by signal PHS3 to reset the branch 1 flip-flop and then by signal PHS4 to set the flip-flop if signal L15 is present.

Control pulse TSGN tests write line WL16 for sign. Control pulse TSGN is first gated by signal PHS3 to reset the branch 1 flip-flop and then by signal PHS4 to set the flip-flop if signal WL16 is present. Signal WL16 is present when the content placed onto the write lines is negative.

Signal BR1 is produced when the branch 1 flip-flop is set. Signal MBR1 is applied to an indicator on the peripheral equipment together with the output of the branch 2 flip-flop. In this manual the content of the two branch flip-flops are referred to as c(BR1, BR2) whereas the indicators on the peripheral equipment display c(BR2, BR1).

The branch 2 flip-flop is used to test plus zero, positive overflow, and minus zero. It is also used to test the sign of one quantity while the branch 1 flip-flop tests the sign of another quantity. It is necessary to determine the sign of two quantities being multiplied together in order to establish the correct sign of the product. The branch 2 flip-flop is always cleared before a net input occurs. Control pulse TPZG tests for plus zero in register G. Control pulse TPZG is first gated by signal PHS3 to clear the branch 2 flip-flop and then by signal PHS4 to set the flip-flop if signal GEQZRO is present.

Positive overflow exists when bits 16 and 15 of a word are 0 and 1, respectively. Positive overflow means that computer word length has been exceeded by a large positive quantity. Signal OVF is present when this condition exists. Control pulse TOV, which also tests negative overflow, is gated by signal PHS2 to clear both branch flip-flops. After the flip-flops are cleared, the branch 2 flip-flop will be set if signal TOV is present.